Proceedings of the Sixth International Conference on Trends in Electronics and Informatics (ICOEI 2022)
IEEE Xplore Part Number: CFP22J32-ART; ISBN: 978-1-6654-8328-5

Performance Evaluation of Auxiliary Threshold Low Power 6T SRAM Cell

Selvakumar G*[1]
Assistant Professor, Department of ECE
SCAD College of Engineering and Technology
Tirunelveli,India
selvakumargeorge@gmail.com

Muthu kumaran S [2]
PG Scholar,Department of ECE
SCAD College of Engineering and Technology
Tirunelveli, India
mkumaran3525@gmail.com

Sathish Kumar N.[3]
Assistant Professor (Sr.G), Department of ECE
KPR Institute of Engineering and Technology
Coimbatore,India
sathishkumar2490@gmail.com

Asirvatham M[4]
Assistant Professor, Department of ECE
SCAD College of Engineering and Technology
Tirunelveli,India
email2asir@gmail.com

Indhumathi R.[5]
Assistant Professor, Department of ECE
Vivekanandha College of Engineering for Women
Tiruchengode,India
Indhuma2228@gmail.com

Ezhil E. Nithila[6]
Assistant Professor, Department of ECE
SCAD College of Engineering and Technology
Tirunelveli,India
enithila@gmail.com

2022 6th International Conference on Trends in Electronics and Informatics (ICOEI) | 978-1-6654-8328-5/22/$31.00 ©2022 IEEE | DOI: 10.1109/ICOEI53556.2022.9777142

***Abstract*—In all digital devices,memories plays significant role. To improve the system performance, power consumption and speed are the major considerations.In current digital world, low power devices need two important operations such as read and write. In this work, CMOS-based 6T SRAM cells are designed and the performance is analysed using different techniques. By using Tanner tool the conventional 6T SRAM , Self controllable voltage level 6T SRAM, and auxiliary threshold 6T SRAM cells were simulated and evaluated. The Proposed method incorporate an auxiliary threshold to conventional 6T cell. When compared with other 6T SRAM cell, this proposed arrangement reduces power and noise level.**

***Index Terms*—6T SRAM cell, Self controllable voltage level, Auxiliary threshold, power reduction, noise reduction.**

I. Introduction

Sensational development in VLSI (Very Large Scale Integration) innovation has expands the thickness of Integrated Circuits (IC) by lessening the device geometries. CMOS technology is fast progressing toward large scale integration on a single chip, resulting in decreasing chip sizes that consume less space [16]–[18]. The inherent density of the chip grows as technologies continue to be down scaled.Lower voltages and more modest size cause critical corruption of information steadiness in cells [15].High Power and more delays (more simulation time) are the two major factors that disappointments various products like gadgets etc [8].

The device which is used to store the binary information is called Memory unit.But it is well known that memory plays vital role in power dissipation phenomenon. From the memory unit the data is acquired for processing purpose,hence no digital system will get complete without memory. Generally, digital system can hold an memory by storing the incoming data, and data can be retrieved from memory to outside world whenever needed. Hence no digital system will get complete without memory.

RAM (Random Access Memory) which is an memory that permits us to access any byte on the chip directly.RAM is utilized in a variety of systems, including computers and communication systems for the purpose of Reading documents, temporary storage and loading application and there are various applications software programs that are used to build digital circuits [1].

In digital logic circuits, (0,1) are the two stable states of semiconductor memory for data storing is termed as SRAM cell. There are variety of applications in which SRAM cells are used as portable devices like mobile phone, camera, automatic electronics, industries..,etc [2]. In high efficient digital system, inclusion of low power design is main issues [10].SRAM cells include a latch which is called as static memory (Do not need refreshment till the power is ON) [11]. An essential SRAM cell is made up of two cross coupled inverters which behave as memory element. Two switches are used to connect these inverters to complementary bit lines . The complementary bit

Authorized licensed use limited to: ULAKBIM UASL - DOKUZ EYLUL UNIVERSITESI. Downloaded on November 08,2022 at 02:49:19 UTC from IEEE Xplore. Restrictions apply.

line is to make interaction with external peripherals outside of the cell as shown in Figure 1. The self controlled voltage level (SVL) SRAM cell was constructed using six transistors, each pair of transistors for driving, NMOS and PMOS. The PMOS and NMOS act as cross coupled inverters. This model has two stable states namely logic 0 and logic 1.

When compared to 4T SRAM cell, the proposed 6T SRAM structure provide enhanced electrical parameters like static noise margin, speed and low power [3].The writing process can be enhanced by cross-coupled inverters [14].

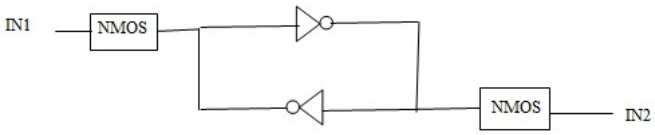


Fig. 1. Basic SRAM cell.

II. Methods

A. Conventional 6T CMOS SRAM cell

The conventional 6T CMOS SRAM cell contains four NMOS (M1,M2,M4,M6) and two PMOS (M3,M5) transistors. The NMOS (M4,M6) and PMOS (M3,M5) transistors operate as cross coupled inverters. The NMOS (M1,M2) transistors act as word select line (WL) as shown in Figure 2.

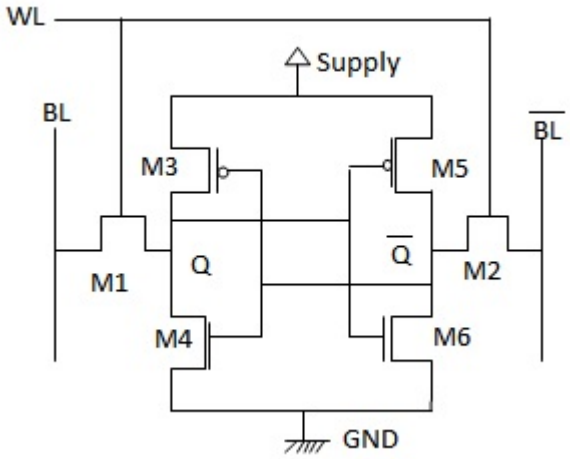


Fig. 2. Conventional 6T CMOS SRAM cell

During the read operation, the word line is activated if and only if bit line (BL) and bit line bar $(\bar{BL})$ are pre-charged. Now the cell will be charged each in state '1' or in state '0'. The voltage difference is found between BL and $(\bar{BL})$ whereas the sense amplifier senses the voltage difference and the bit available in the line will be displayed at the sense amplifier output. During read operation the bit signal is generated from input data and bit bar signal is nothing but the complementary of input data. The word line is then asserted, turning on the two NMOS transistors and writing the data into the cell [5]. During the write operation, before the voltage is applied to word line the bit line and bit line bar should be supplied with complimentary values. A pass transistor will discharge the node that stored the zero value in n ideal or standby state. The connection between internal nodes and bit lines is not made. If the power is given, the inverters act as a storage element, reinforcing the data bit within the cell [4].

There are two types of power dissipation that affect SRAM cells. One is related to dynamic power, and the other is owing to the MOS transistor's leakage current.Conventional small size 6T SRAM cell exhibit low stability with minimum supply of power. During the read activity, the steadiness radically diminishes because of the voltage division between M1 and M2 transistors [8]. Therefore implementing a self-controllable voltage level (SVL) [6] can alleviate the above mentioned dynamic power and leakage current issues.

B. SVL in 6T SRAM cell

The designed self-controllable voltage level (SVL) circuit may supply low DC voltage to an active load circuit on standby mode or peak DC voltage to a load circuit in standby mode. The designed SVL circuit exponentially decreases the leakage power irrespective of speed and size of the chip. It can be applied to memory or register because SVL is capable of store data even in stand by mode.

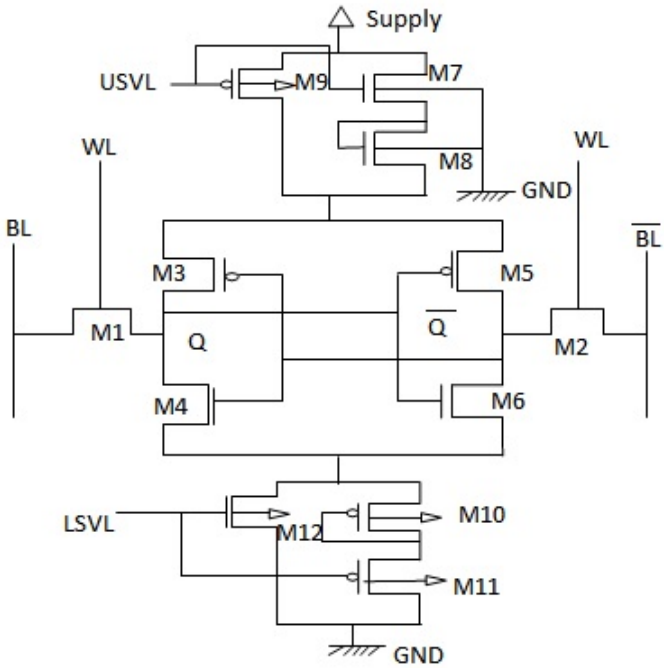


Fig. 3. Self-controllable voltage level in 6T CMOS SRAM cell

Two sets of SVL circuits are connected in the SRAM cell, one connected above the two PMOS (M3, M5) and the other connected below the two NMOS (M4, M6) as shown in Figure 3. The first set of USVL (upper SVL)circuits

Authorized licensed use limited to: ULAKBIM UASL - DOKUZ EYLUL UNIVERSITESI. Downloaded on November 08,2022 at 02:49:19 UTC from IEEE Xplore. Restrictions apply.

connected above the 2 PMOS transistors consists of two series-connected NMOS (M7, M8) in parallel with the single PMOS (M9) structure. PMOS(M9) and NMOS (M7) are the pull up transistors which are used for power gating that cuts off the power which was established for the activation of SRAM cell. Under such condition leakage is reduced. The mode which we follow such type of power measurement is known as static power. The second set of LSVL (lower SVL) which was connected below the 6T SRAM cell consists of two series-connected PMOS (M10, M11) in parallel with the single NMOS (M12) structure.The pull down transistors in the LSVL causes an rise in ground voltage. This decreases the gate-drain voltage and gate-source voltage making SRAM cell to move under OFF state and SRAM cell goes on when gate-drain voltage increases [**?**]. These results in reducing leakage gate current and hence reduce static power dissipation. The width of the transistor positioned at the top of SRAM is termed as upper SVL circuit controls the MOS transistor's impedance. There will be large resistance path across Vd and supply if the transistor M9 is widen. In normal mode of operation, the read and write pair was formed by the transistors M7 and M8. In active mode, the top SVL circuit reduces the current and leakage power as transistor M8 act as resistor. If the width of the transistor in a LSVL circuit increases then MOS transistor's impedance increases. The impedance of a MOS transistor grows with the width of the transistor in a lower SVL circuit. If M12 is wide, it provides high impedance in the path between supply and Vd. In the cell M12 works in SVL mode whereas M10 and M11 works in normal mode. In order to reduce leakage power M10 acts as a resister. Such arrangement establishes a threshold and reduces the current thereby reducing the power to a certain extent. The power can also be reduced further by introducing an auxiliary threshold in the circuit.

C. Auxiliary threshold in 6T SRAM cell

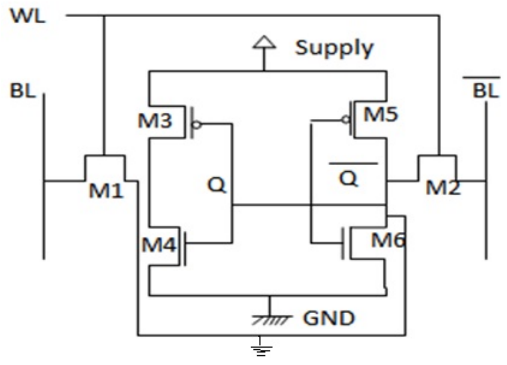


Fig. 4. Auxiliary threshold in 6T CMOS SRAM cell

There are many power minimizing procedures like multi edge voltage CMOS and variable edge CMOS [12]. Even though these techniques reduce power, auxiliary threshold voltage reduces more power when compared to previously defined. Auxiliary threshold 6T SRAM is presented in Fig. 4, it has single end write function [6]. There is a significant increase in noise margin due to read path which is isolated from storage nodes. The leakage power was reduced by M1 transistors arrangement which is used to read cell data [7].

III. Experimental Results and Discussion

Tanner EDA is an suitable tool for designing if integrated circuits. This is an leading and powerful tool used by many industries. Using Tanner tool schematics, SPICE simulations and layout design can be achieved [20]. The proposed work uses Tanner EDA version 16.3 tool for obtaining simulation result.

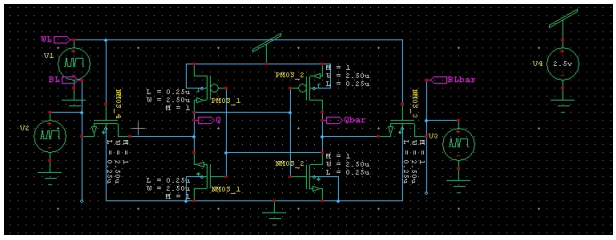


Fig. 5. Schematic diagram of Conventional 6T SRAM cell

The simulation waveform in figure 6 shows Read/Write operation of SRAM Cell. In all cases BL,($\bar{BL}$), WL are taken as input, Q, Qbar is taken as output. The SRAM cell first writes the data '1' and the data gets stored in the memory. For write cycle, word lines go high as shown in the waveform. Under such condition the output goes high. When data goes to '0', the output will also goes to '0'. Traditional 6T SRAM cell Schematic diagram is depicted in Figure 5.

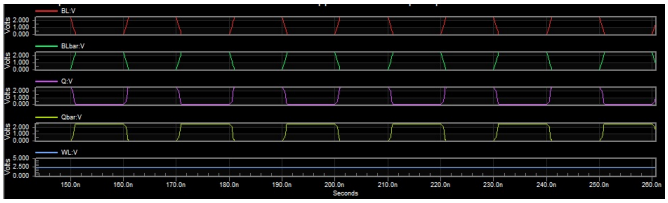


Fig. 6. Output of Conventional 6T SRAM cell

Figure 7 depicts the Schematic diagram of an SVL in 6T SRAM cells. Figure 8 depicts the Output of the SVL in 6T SRAM cells.Figure 9 depicts the schematic diagram of an Auxiliary Threshold in 6T SRAM cell. Figure 10 depicts the Output of the Auxiliary Threshold in 6T SRAM cells.

Table 1. depicts the comparison between conventional 6T SRAM, SVL in 6T SRAM and Auxiliary Threshold in 6T SRAM cells. The comparison chart shows that power and latency of Auxiliary Threshold in 6T SRAM cell was very much minimized when compared with conventional 6T SRAM cell. Performance measures are calculated in terms of power dissipation, delay, and evaluation time. It was shown that the proposed SRAM cell outperforms well when compared with other simulated results.From Figure 11, it was evident that proposed SRAM cell dissipates lesser power, delay, and run-time than the other two SRAM cells.

Authorized licensed use limited to: ULAKBIM UASL - DOKUZ EYLUL UNIVERSITESI. Downloaded on November 08,2022 at 02:49:19 UTC from IEEE Xplore. Restrictions apply.

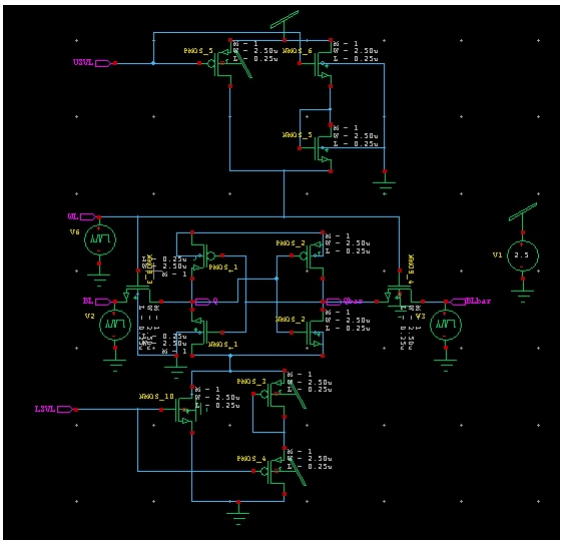


Fig. 7. Schematic diagram of SVL in 6T SRAM cell

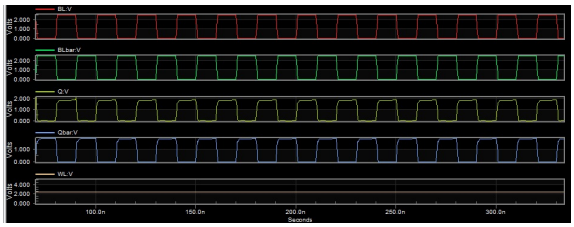


Fig. 8. Output of SVL in 6T SRAM cell

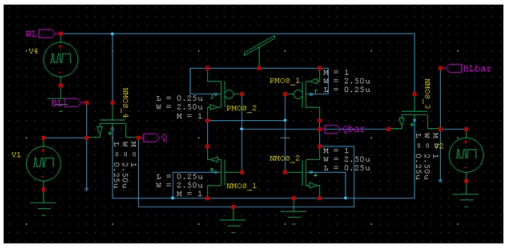


Fig. 9. Schematic diagram of Auxiliary Threshold in 6T SRAM cell

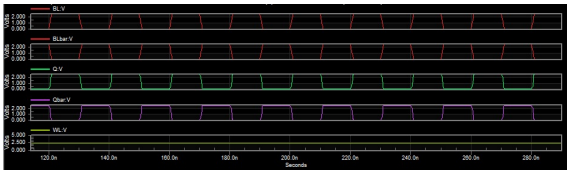


Fig. 10. Output of Auxiliary Threshold in 6T SRAM cell

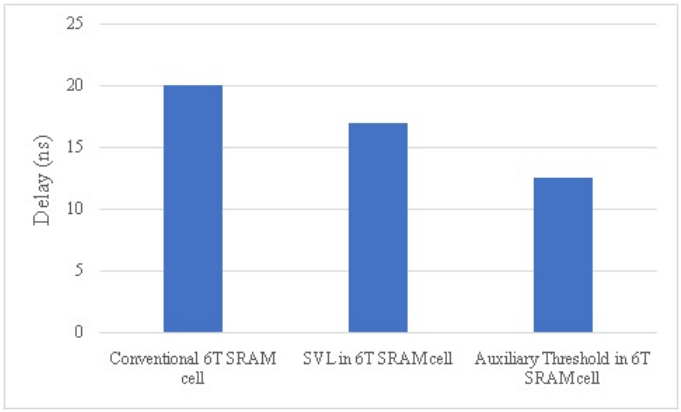


Fig. 11. Performance Evaluation in terms of Delay

The Overall efficiency of the 6T SRAM cell can be determined by the product of Power and Delay. If the product of Power and delay are very less, then the cell can be considered as energy efficient [21]. In our proposed method, Power Delay product is less compared to previous methods. Proposed circuit uses multiple transistors. Each transistor has different threshold voltage. The threshold voltage is formed at the gate terminal of the MOSFET (Metal Oxide Semiconductor Field effect Transistor) which interfaces between oxide layer and substrate layer. High threshold voltage which is produced between them reduces the leakage power and delay. From the output, it can be visualized that the output can be generated without delay. For reading the cell data, transistors M1 used. By connecting transistor to virtual ground standby leakage can be minimized.

In Our proposed work different methods were analysed to reduce delay and power of the SRAM cell. Utilization of noise level by the cell and its elimination can be performed using Static Noise Margin analysis which is to be focus on our future work.

TABLE I
COMPARISON OF CONVENTIONAL METHOD WITH THE PROPOSED METHOD

Sl No	Methods	Power(micro watts)	Delay(ns)	Run Time(s)
1	Conventional(6T)	70	20.1153	1.18
2	SVL(6T)	35.71	17.0596	1.04
3	Auxiliary Threshold(6T)	17.86	12.5997	0.74

IV. CONCLUSION

The proposed 6T SRAM cell with auxiliary threshold reduces delay upto 5ns. The proposed design also reduces the power consumption to 70 percent and 50 percent when compared to conventional 6T SRAM and self controllable voltage level (SVL) respectively .The speed of designed system increases reasonably as shown in Table 1. Hence it is

Authorized licensed use limited to: ULAKBIM UASL - DOKUZ EYLUL UNIVERSITESI. Downloaded on November 08,2022 at 02:49:19 UTC from IEEE Xplore. Restrictions apply.

concluded that the 6T SRAM cell with auxiliary threshold is better choice for high speed applications in memory elements.

REFERENCES

[1] Akshaya.N, Bini Joy, SathiaPriya.M, Arul Kumar.M, Design of SRAM Cell by Using Self-Controllable Voltage Level Circuits, International Journal of Innovative Research in Computer and Communication Engineering, 3(2), (2015), pp.708-714
[2] M. Devi, C. Madhu and N. Garg, Design and analysis of CMOS based 6T SRAM cell at different technology nodes, Materials Today: Proceedings,https://doi.org/10.1016/j.matpr.2020.05.130.
[3] S. Banu, S. Yogesh, R. Kamalam, Design of Low Power 6T SRAM 8 * 8 ArrayUsingGateway Transistor, International Journal of Advanced Research in Education Technology, 2 (2015) 125–128
[4] P. Raikwal, V. Neema, A. Verma, Design and analysis of low power single ended 8T, in: SRAM ARRAY (44) at 180nm technology, in: 2016 International Conference on Signal Processing, Communication, Power and Embedded System (SCOPES), IEEE, 2016, pp. 312–316,
[5] Varun Kumar Singhal, Balwinder Singh, —64 bit low power CMOS SRAM by using 9T cell and charge recycling schemell, International Journal of VLSI design Communication Systems (VLSICS) Vol.2, No.7, June 2011.
[6] Brews, J. (1990). High speed semiconductor devices (pp.139–210). New York: Wiley
[7] K. Gavaskar, U. S. Ragupathy, Low power self-controllable voltage level and low swing logic based 11T SRAM cell for high speed CMOS circuits, Analog Integrated Circuits and Signal Processing, 2018.
[8] Budhaditya Majumdar, Sumana Basu, Low power single bitline 6T SRAM cell with high read stability, Conference: 2011 International Conference on Recent Trends in Information Systems, December 2011.
[9] Rajnarayan Sharma, Ravi Antil, Kamlesh Kumar, Comparative Study of 6T and 8T SRAM Using Tanner Tool, IJCSMC, Vol. 4, Issue. 1, January 2015, pg.211 – 221.
[10] International Technology Roadmap for Semiconductors.[Online].Available:http://public.itrs.net.
[11] Ankita Chauhan; D.S Chauhan; Neha Sharan , Characterization of 6T CMOS SRAM in 90nm Technology for Various Leakage Reduction Techniques, 2016 IEEE ' Conference on Electrical, Electronics and Computer Science.
[12] Dawoud, Dawoud Shenouda, and R. Peplow. Digital System Design: Use of Microcontroller. Vol. 2. River Publishers, 2010.
[13] Prerna Chauhan, Bal Krishan, Design and implementation of low power SRAM cell using self-controllable voltage level, International conference on Emerging Trends in Engineering, Technology, Science and Management, June 2017.
[14] Chang-Hoon Choi, Ki-Young Nam, Zhiping Yu, R.W.Dutton (2001), "Impact of Gate Direct Tunneling Current on Circuit Performance: a Simulation Study," IEEE Transactions on ED, vol. 48, no. 12, pp. 2823-2829
[15] Takeda, K.; Hagihara, Y.; Aimoto, Y.; Nomura, M.; Nakazawa, Y.; Ishii, T.; Kobatake, H. A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications. IEEE J. Solid-State Circuits 2006, 41, 113–121
[16] Anand A., Selvakumar G. (2016), "Reliable and Efficient Multicast Protocol for MPEG-4 Transmissions over IEEE 802.11n", International Journal of Computer Science and Mobile Computing, Vol.4, No.11, 344-349, ISSN 2320–088X.
[17] Dr. Nandalal V., Selvakumar G., (2017), "Power Optimization in OFDM Networks using various Peak to Average Power Ratio Techniques" Asian Journal of Applied Science and Technology (AJAST), Vol.1, No.2, pp. 185-199, ISSN 2456-883X.
[18] Selvakumar G., Anand A. (2016), "Spectral Efficient IDMA System Using Multi User Detection", International Journal of Scientific and Technical Advancements (IJSTA), Vol.2, No.1, 49-52, ISSN 2454-1532
[19] Torrens.G, Alorda.B "Adaptive static and dynamic noise margin improvement in minimum sized 6T SRAM cells", Microelectron. Reliab, 11, pp. 2613-2620, 2014.
[20] Tanner EDA, http://www.tannereda.com/.
[21] Shikha Saun and Hemant Kumar 2019 , Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization ,IOP Conf. Ser.: Mater. Sci. Eng. 561 012093

Authorized licensed use limited to: ULAKBIM UASL - DOKUZ EYLUL UNIVERSITESI. Downloaded on November 08,2022 at 02:49:19 UTC from IEEE Xplore. Restrictions apply.