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Analysis of Full Adder cells in Numerous Logic Styles

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***Abstract*— In this electronic design age, there is always a quest for improved performance digital integrated circuits (ICs) in most of the application areas of electronics and communication. Complex arithmetic and logic circuits accommodated with multipliers and adders always occupy larger areas inside the ICs. Since, when calculations are composed for the execution of the application circuits including these ICs, duplication, and expansion tasks are dominating. Hence, in order to plan a better exhibition of full Adder cells in the main stage, an investigation of low-region possessing and low-power-consuming adders acknowledged in CMOS rationale, pass semiconductor rationale (PTL), and transmission entryways (TG) rationale is planned. To get non debased rationale level results, transmission entryways (TG) are reasonably obliged in the PTL based plans. Subsequently, also with CMOS-based 28 semiconductors (28T), PTL with TG based 16 semiconductors (16T), and PTL with TG based 14 semiconductors (14T) full Adder cells are gotten. At long last, productive format planning is done in all the above renditions of full Adder cells with fixation of having further developed execution. The reenactment consequences of CMOS based on 28 semiconductors (28T), PTL with TG based on 16 semiconductors (16T), and PTL with TG based on 14 semiconductors (14T) full adder cells are acquired. The presentation examination of the full Adder cell in these rationale styles uncovers that Pass Transistor Logic incorporates Transmission Gate based 16T full Adder cell has 85.8% of force utilization improvement contrasted with the full Adder cell with CMOS rationale. Thus, this adaptation of the full Adder cell can be used for applications requiring decreased power utilization. Additionally, the Pass Transistor Logic incorporates Transmission Gate based 14T three input Adder has a lower word related region than that of the other two adaptations**

Keywords— Pass Transistor Logic, Transmission Gate, Full Adder , PTL-TG, VLSI, and Conventional CMOS Logic

I. INTRODUCTION

VLSI technology is the most promising technology in this contemporary era. Designing digital Integrated Circuits with improved performance full adder cells is essential for most of the electronics and communication-based application circuits are considered. Most generally, in practically all processors, math and rationale units with multipliers, dividers, modulators, logarithmic speakers, recollections, and so on, are the significant components[10]. Most likely, the circuits inside these squares have the full Adder as their fundamental component [1][11]. Henceforth, to get the general power streamlining in a VLSI IC, as an underlying endeavor, the power decrease in full adders is the strong point of the VLSI originators [8].

Seeking after the plan with more elevated levels of deliberation, specifically, algorithmic and building levels for each sub-circuit of a VLSI IC prompts expanded intricacy. Addressing the required subcircuits in any of the advantageous lower levels of deliberation, to be specific, circuit, rationale, and semiconductor levels are finished easily with the assistance of the guidance arrangements of equipment depiction language (HDL). Consequently, to have an effective methodology of execution of the application circuits inside the VLSI IC, the equipment depiction language gives numerous decisions for portraying, orchestrating, and confirming the plans with decreased intricacy.

The decrease in the silicon region during creation prompts a decrease in power utilization. Accordingly, picking less energy taken in the intelligent plan stage and working on the productivity of the actual plan stage by taking on the improved situation and steering methods gives very poor energy with diminished spread deferral. With this discernment, the plan and execution adder was completed by choosing the low-power consuming rationale styles, for example, Conventional Logic 28 T adder[2], Pass transistor logic incorporate with Transmission gate 14 T and 16 T adder. The less region possessing and low power consuming rationale styles are portrayed in Section II. Segment III expounds the effective full Adder cell configuration approaches with these rationale styles which have been intended to have legitimate clamor edges and to have the completely level re-establishing capacities. In Section IV, recreation results of the planned full Adder cells with the considered rationale styles are shown alongside their separate area and power utilization results[12]. Segment V gives the finish to this work.

II. LOGIC STYLES

A. Pass Transistor Logic

In the CMOS logic style, fixed power supply voltage levels, namely +5 volts and 0 volts are used for representing

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the logic level input signals. When the logic signal passes through the subsequent stages connected in series, the required non-degraded logic level will be maintained at each output node. But in PTL, instead of feeding the required logic level input from the power lines, the source region of the single NMOS or PMOS transistor is fed with the required logic level input [5]. As the no degraded logic level signal passes through the serially connected NMOS or PMOS transistor stages, between each transistor's drain and source the signal level is progressively deteriorated and thus drops below the threshold voltage level. In order to restore this degraded voltage level at each gate output; sufficient level restoring circuits are needed. Also, in PTL, is given correct output, gate output is attached inverters.

In the pass transistor logic representation shown in fig. 1, depending on the input signal (either logic "1" or logic "0"), the transistor is used as a high-low pulse equivalent to the switching pin used to drop down or top up the charge in the parasitic capacitance that exists at its output.

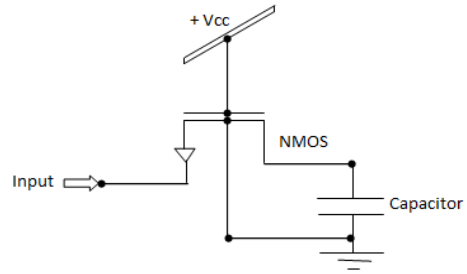


Fig. 1. Pass transistor Logic.

In either case, the output of the NMOS transistor assumes a logic-low or logic-high signal level, depending upon the input logic level signal applied.

B. *Transmission Gate*

The structure of the transmission gate or analog switch is given in Fig. 2. It selectively blocks or passes the signal level from its input to output. The CMOS transmission entryway comprises of two MOSFETs, one n-channel answerable for the right transmission of rationale 0's and one p-channel answerable for the right transmission of rationale 1's. There is no seclusion between the information and the result. The result dynamically weakens as it goes through different stages when combinational rationale circuits are executed in this rationale style.

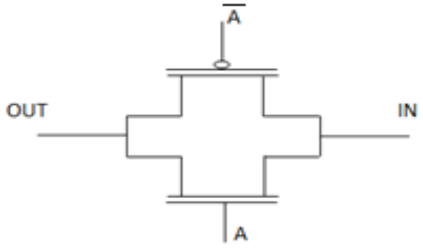


Fig.2. Transmission Gate.

C. *Standard CMOS Logic*

In conventional CMOS logic, the PMOS constructed with a pull-up network and the NMOS constructed with a pull-down network is connected between the constant voltage source and the output of the gate network. The basic block for the conventional CMOS logic is shown in Fig. 3.

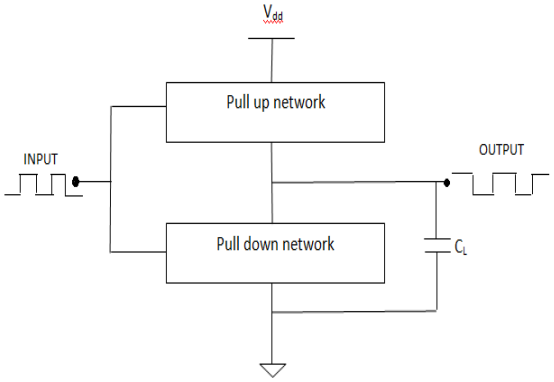


Fig. 3. Conventional CMOS Logic

1) *Energy dissipation in CMOS logic*

The charge has driven from the power supply during the charging phase (Q) = $\frac{C\ load}{Vdd}$. At the end of this charging phase, the stored energy in the load capacitor (CL) is E = $\frac{1}{2}$ CL Vdd2 [7][9].
This shows that, out of the absolute energy drawn from the power supply, a large portion of the energy is disseminated in the PMOS organization and the leftover portion of the energy is put away in the heap capacitor (CL) as represented in Fig. 4. The resistor R is the equivalent resistor representing the PMOS pull-up network.

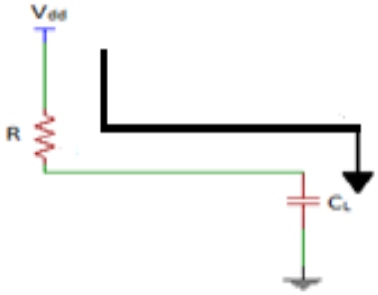


Fig.4. Charging process in CMOS Logic.

During the releasing stage, the energy put away in the heap capacitance is scattered in the NMOS pull-down network Fig. 5 shows this discharging path of the current through the NMOS network which is equivalently represented as a resistor R[4][14].

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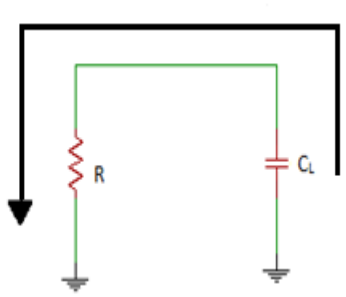


Fig.5. Discharging process in CMOS Logic

The total energy dissipated during the charging and discharging phases is, E = CL Vdd2.

III. Full Adder Cell Organization

A. *Regularly based 28T-CMOS*

The convention logic complementary metal oxide semiconductor using 28 Transistor [13] is shown below logic Fig. 6. The pull-up and pull-down circuit channel points between the source and drain (W/L). The proportionate ratio of (W/L)= (2µm/0.12µm).

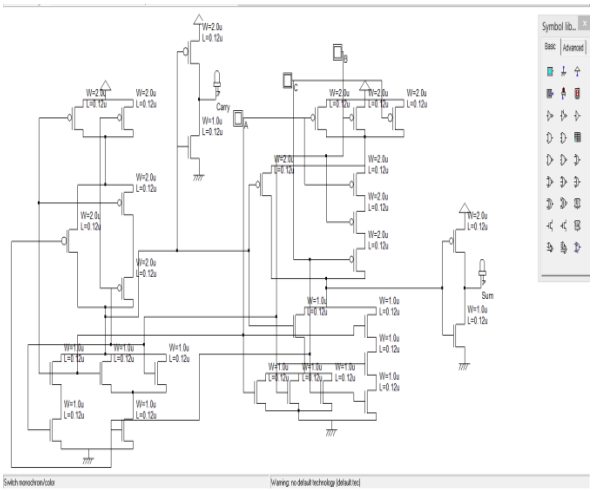


Fig.6. Regular based 28 T-CMOS

B. *Pass Transistor rationale related to transmission Gate*

Transmission gates are the completely reestablished rationale rendition of PTL whose yield rationale level doesn't debase while passing the separate rationale level sign accessible on its bits of feedback. Thus, in planning the Pass Transistor logic FA, to get the non-corrupted results of aggregate and convey, TG is appropriately embedded in the plans [3].

1. *16T Pass Transistor Logic incorporates Transmission Gate*

The pass semiconductor rationale (PTL) and transmission entryway (TG) with 16 semiconductors full Adder cell are displayed in Fig. 7. The final value of this designed adder gives better results compared to conventional 28 T – FA.

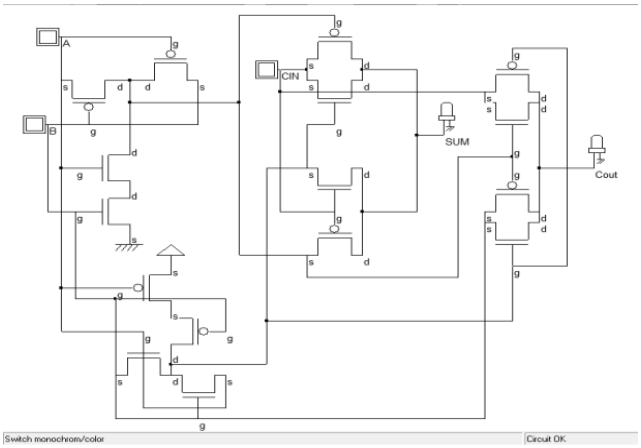


Fig.7. 16 Transistor Designed Modified Architecture

2. *14T Pass Transistor Logic incorporates Transmission Gate*

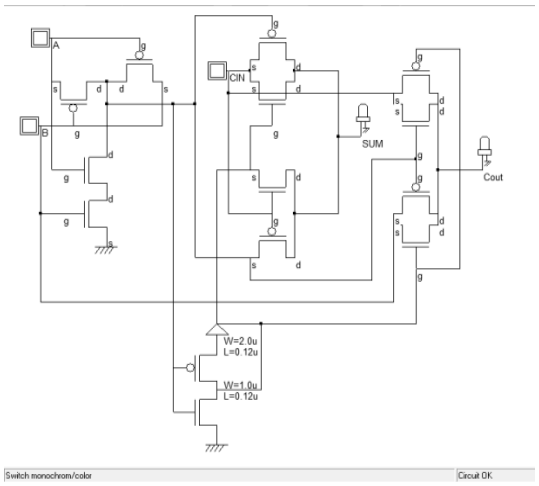


Fig. 8. 16 Transistor Designed Modified Architecture

This architecturally reduced count of transistors from 16T to 14T is shown in diagram Fig. 8. The count reduced this level of output is better performance compared to previous one.

IV. Design Verification of Full Adder Cells

A. *CMOS based 28T Full adder cell*

The resulting waveform of CMOS-based full Adder cell utilizing 28T is displayed in Fig.9. The results are addressed to Sum and Cout. During the initial no good length, the data sources given and the comparing yields acquired are 1) A=0, B=0, C=0 and Sum =0 and Cout =0. 2) A=0, B=0, C=1 and Sum =1 and Cout=0.

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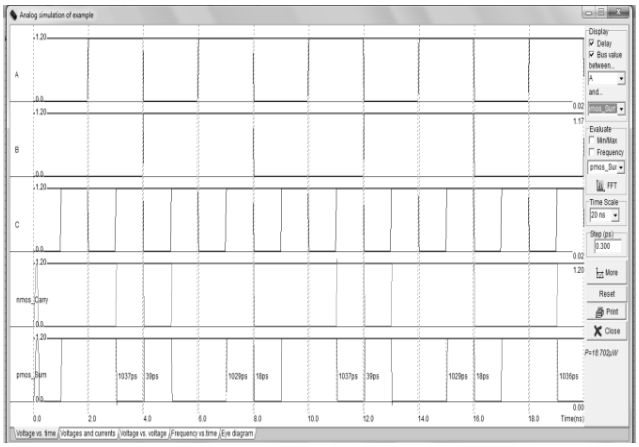


Fig.9. CMOS-based 28T full adder simulation output waveform.

The rationale check completed for one explicit information mix is shown in Fig. 10. The given sources of info are A=1, B=1, and Cin=0 and the aggregate and Cout for this reproduction are rationale '0' and rationale '1' individually[15].

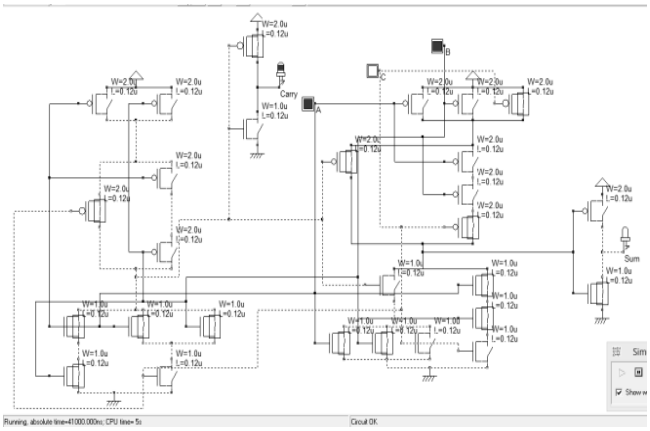


Fig. 10. CMOS-based 28T full adder simulation output.

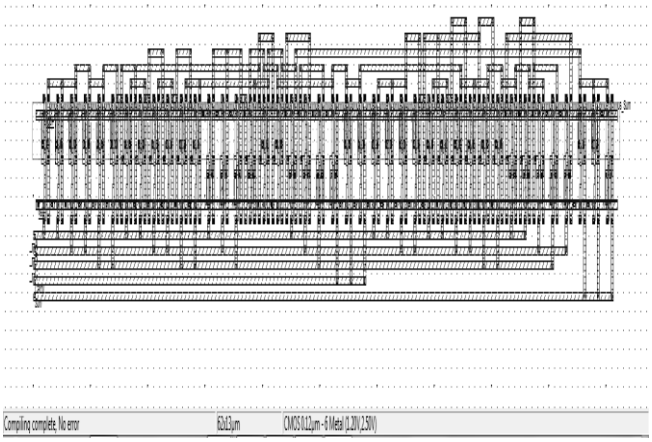


Fig.11. 28T-CMOS adder layout.

The layout view of the Complementary MOS 28T design is given in Fig. 11. This output occurs 0.12µm duty cycle, it consumes 1.2V power supply. At the level of 6 metal layer is used in planning interaction [6].

B. PTL- TG Integrated 16T Adder

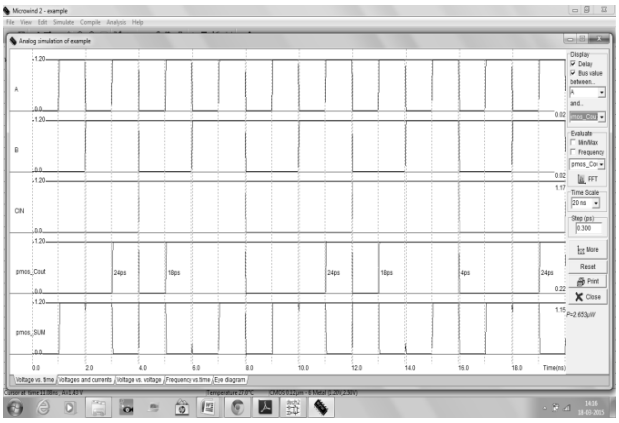


Fig.12. 16T FA cell Simulation waveform.

The resulting waveform of 16T logic full Adder cell is displayed in Fig.12. The results are addressed as Sum and Cout. During the initial good for nothing terms, the sources of info given and the relating yields acquired are 1) A=0, B=0, C=0 and Sum =0 & Cout =0. 2) A=1, B=0, C=0 and Sum =1 & Cout=0.

The rationale confirmation completed for one explicit information mix is represented in Fig. 13. The given sources of info are A=1, B=0, and Cin=1 and the aggregate and Cout for this recreation are rationale '0' and rationale '1' separately.

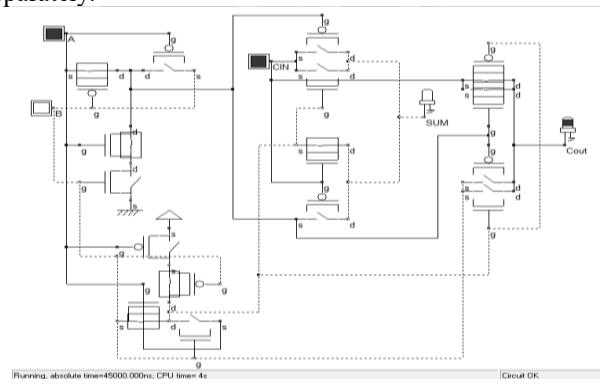


Fig.13. PTL-TG Integrated 16T Adder

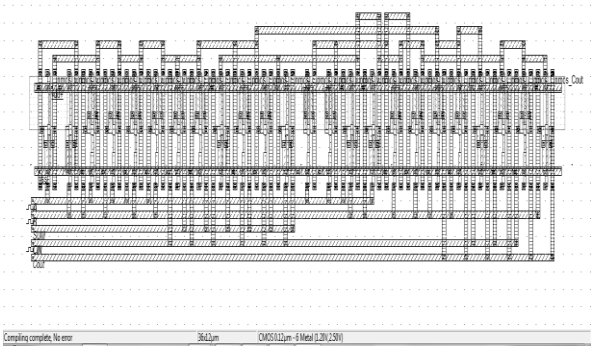


Fig. 14. 16T logic Layout diagram

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The above-mentioned circuits operate with a voltage of 1.2V. Its occupied cross-section of the metal layer which is consist of 6 [9].

C. PTL- TG Integrated 14T Adder

The resultant waveform of 16T modified logic adder is displayed in Fig.15. The results are addressed as Sum and Cout. During the initial, no good spans, the sources of info given and the comparing yields acquired are 1) A=0, B=0, C=0 and Sum =0 and Cout =0. 2) A=1, B=0, C=0 and Sum =1 and Cout=0.

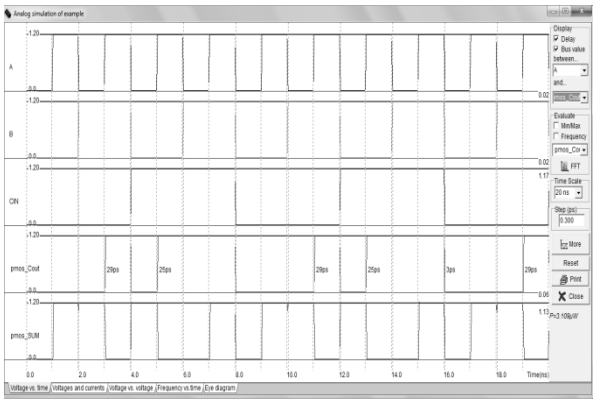


Fig.15.PTL-TG Integrated 14T Adder

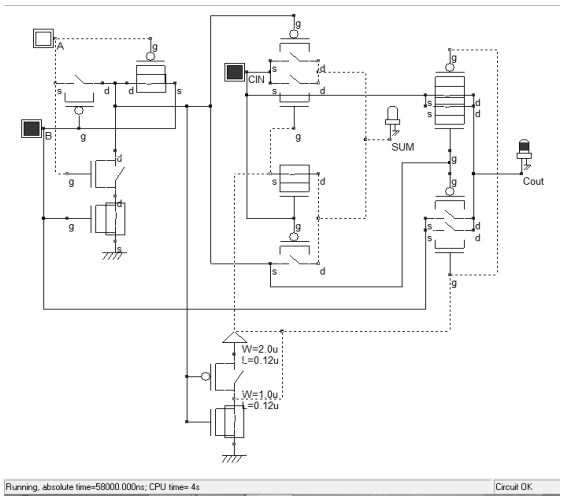


Fig.16. PTL-TG Integrated 14T Adder simulation output.

The rationale check completed for one explicit information mix is represented in Fig. 16. The given information sources are A=0, B=1, and Cin=1 and the total and Cout for this reenactment are rationale '0' and rationale '1' separately.

The 14T full adder cell format is given in Fig. 17. This output occurs 0.12µm duty cycle, it consumes 1.2V power supply. At the level of 6 metal layer is used in planning interaction.

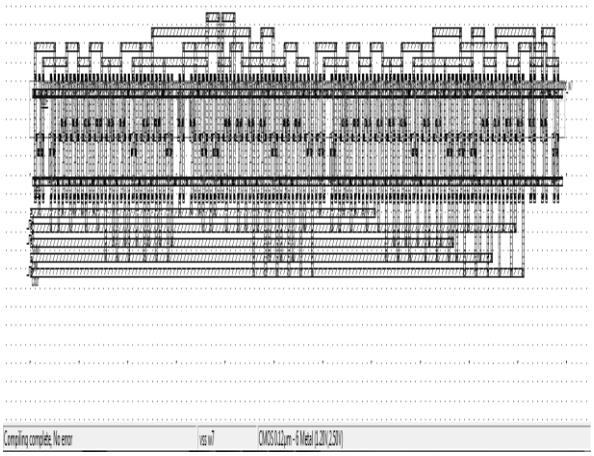


Fig.17. PTL- TG Integrated 14T Adder layout.

V. PERFORMANCE CONSUMPTION ANALYSIS

A. CMOS based 28T Full adder cell

The 28T-CMOS full adder cell involves a design area of 806(µm)^2. The delineation of noticed varieties of force utilization and engendering delay in CMOS-based 28T full adder cell is given Fig. 18.

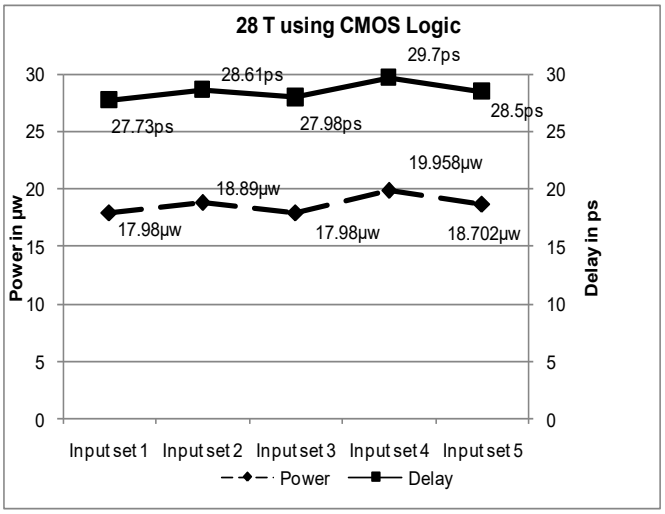


Fig. 18. 28T Adder Graphical illustration of the variation in power consumption and propagation

B. PTL-TG Integrated 16T Adder

The region control of the PTL-TG Integrated 16T Adder is 432(µm)2. The outline of noticed varieties of force utilization and spread deferral in PTL with TG utilizing 16T full adder cells is given in Fig. 19.

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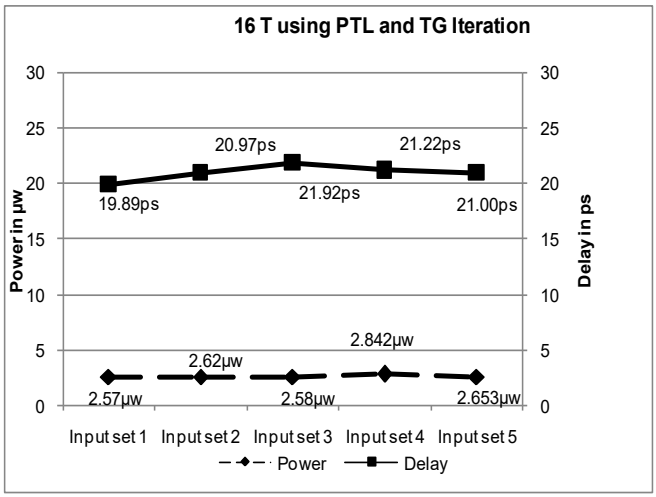


Fig.19. 16T Adder Graphical illustration of the variation in power consumption and propagation delay

C. PTL-TG Integrated 14T Adder

The region controlled by the PTL-TG Integrated 14T Adder is 384(mm)2. The outline of the noticed varieties of force utilization and engendering delay in PTL-TG Integrated 14T Adder is given in Fig. 20.

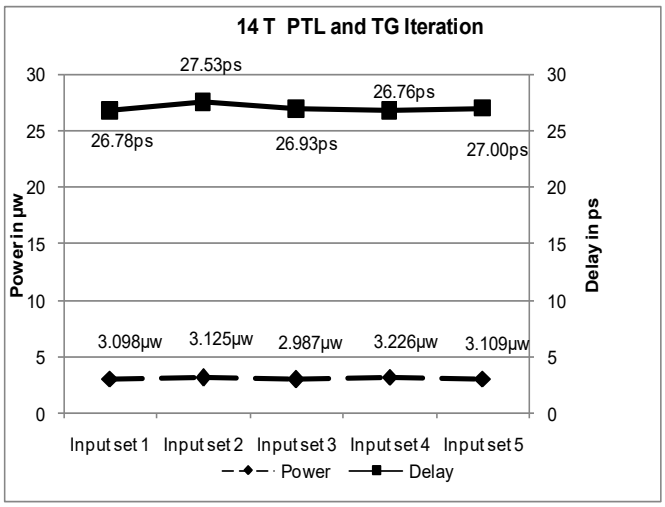


Figure 20: 14T Adder Graphical illustration of the variation in power consumption and propagation delay

D. Power Analysis of Different logic Adder

Table 1, lists the power consumed by the Complementary based Metal oxide semiconductor logic and Modified 16T & 14T logic Adders.

Table 1: Performance summary (measurements)

No of transistor	Power	Area
28 T using CMOS Logic	18.702µw	806(µm)2
16 T using PTL and TG	2.653µw	432(µm)2
14 T using PTL and TG	3.109µw	384(µm)2

The bar diagram which supports looking at the Power and Area of the relative multitude of adaptations of full Adder cells is displayed in Fig. 21 and Fig. 22 separately.

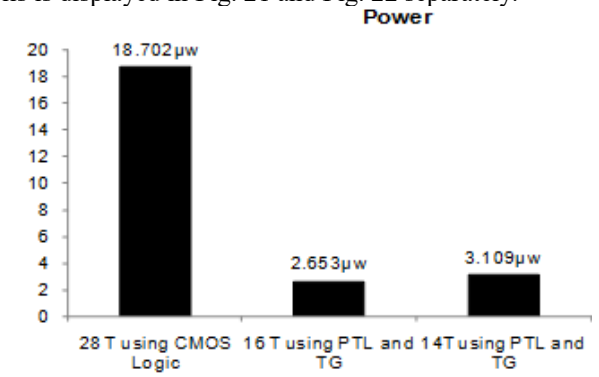


Fig.21. Power comparison Chart

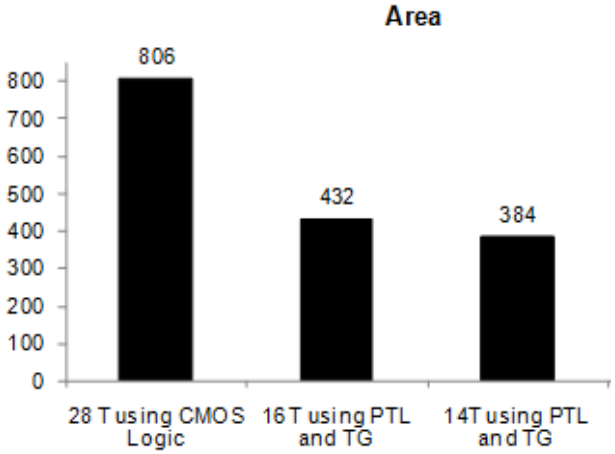


Fig.22. Area comparison Chart

VI. Conclusion

Meaning to carry out a superior execution full adder cell appropriate for implanting inside the computerized ICs, this paper gives a thought of using a better power-consuming full Adder cell or a lesser region involving full adder cell any place required. At the legitimate planning stage, upgraded philosophies are taken on to reestablish the rationale levels when more than one cell is associated in series. Additionally, powerful format plan techniques are embraced in every one of the renditions of full adder cells. The 0.12µm cycle with 6 layer metal is used in all the full adder cell plans. The power utilization of PTL-TG

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Integrated 16T Adder is abundantly decreased contrasted with different renditions. The exhibition examination of the full adder cell in these rationale styles uncovers that PTL-TG Integrated 16T Adder has 85.8% of force utilization improvement contrasted with the full adder cell with CMOS rationale. The region control of PTL-TG Integrated 14T Adder is a lot slower than the other two forms; specifically, CMOS rationale and PTL-TG Integrated 16T Adder

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