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Design of nine step switched capacitor multilevel inverter and its cascaded extension

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Summary

Conventionally, multilevel inverter topologies require components like boost converter, voltage balancing circuits in addition to its switches and gate driver circuitry resulting in increased complexity. A new multilevel inverter topology using the concept of switched-capacitor (SC) is proposed in this article. The basic structure capable of generating 9 level (9L) output voltage waveform with magnitude twice the input voltage at its terminals is proposed. Further, two identical structures are cascaded horizontally to attain 17 level (17L) based on structural modification is suggested. Simulation results are used to analyze the performance of the proposed 9L-SCMLI and 17L-SCMLI in the aspects of total harmonic distortion, R, RL, and dynamic loading conditions. The 9L-SCMLI prototype model is developed to validate the adaptability of the proposed system.

KEYWORDS

9L-SCMLI, 17L-SCMLI, multilevel inverter, switched capacitor, voltage-balancing circuits

1 | INTRODUCTION

In recent years, the world is moving towards renewable energy sources for harnessing electric power. This scenario motivated the researchers to develop suitable technology to extract high-quality power from renewable energy sources like photovoltaic systems.[1–4] The PV system involves two stages of conversion: first, DC-DC and second, DC-AC power conversion.[4–6] In DC-AC power conversion, to get an ac waveform, conventional two-level voltage source inverters[7,8] are employed, which in turn require bulk filters at the output side to reduce the harmonics.

Researchers have developed new configurations to replace conventional two-level inverters with multi-level inverter (MLI).[9] The MLI can generate staircase output voltage waveform closer to sinusoidal waveform providing low electromagnetic interference[10–12] and low device stress with an increased number of levels.[13–15] The inherent property of MLI finds numerous applications in the areas of high voltage medium power applications, which employ a solar PV system. The traditional MLI topologies have disadvantages like the requirement of multiple DC sources and passive elements to synthesize multiple levels. In addition, sensors are required to attain voltage balance among the capacitors.[16] Recent literature shows the development of converter topologies like T type, Hybrid MLI,[17] Active Neutral Point Clamped (ANPC) inverter,[18,19] and SCMLI[20] by modifying the structures of classical topologies to increase the number of levels, reduce the switch count, and achieve inherent capacitor voltage balancing and voltage boosting. Several hybrid multilevel inverter topologies like Flying Capacitor–Cascaded H Bridge (FC-CHB), Neutral Point Clamped–Cascaded H

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Bridge (NPC-CHB), and Neutral Point Clamped–Flying Capacitor (NPC-FC)[21–24] developed by combining traditional topologies have not been proved useful for low and medium power application.

Among the novel topologies, SCMLI has been widely accepted, and various topologies have been proposed in recent times. The switched capacitor structure is used to create the required AC voltage level using active switches, diodes, and capacitors. Series–Parallel SCMLI[25] possessing a compact structure and reduced switch count capable of generating more levels with its extended structure. In a previous study,[26] a nine-level two-stage topology comprising three capacitors switched in series/Parallel connection, a single DC input source and 13 active switches are suggested. In the literature,[27–29] a ladder-type SC structure is presented but requires more number of bidirectional switches and DC source for synthesizing a higher number of output levels. A two-stage nine-level SCMLI[27] with a boosting ability of 1:2 and employing 10 switches is proposed with H-Bridge Circuit connected at the backend for polarity conversion, but the drawback in the H bridge is that the switches have to withstand the voltage twice the input voltage. Reza et al.[28] prepared several simulation models for a new boost switched-capacitor multilevel converter with reduced circuit devices. Two isolated DC sources were utilized for the operation of switches and the magnitude of voltages adjusted based on the symmetric/asymmetric types of configurations for synthesizing maximum levels. A single-stage switched capacitor module topology for cascaded multilevel inverters[29] is developed which eliminates the drawbacks of a two-stage module, this design ultimately reduces the number of isolated DC sources when compared with cascaded H bridge inverters, but a number of switches in the conduction path and the total standing voltage are considerably high. Samadaei et al.[30] created a new configuration of a 13 level multilevel inverter with two unequal DC sources. This circuit utilizes 14 semiconductor switches and four diodes with two switching capacitors. Based on the early literature, the proposed work intends to develop single-stage topology encompassing all the merits of SCMLI[29–33] with reduced switch count. The feasibility of adopting the inverter under R load, RL load, and dynamic loading have been analyzed using high-frequency operation.

The key contributions of the proposed topology are

- nine-level inverter with fewer switching components;
- inherent voltage balancing ability and a boost factor of 200%; and
- it can be cascaded to generate 17 levels and 49 levels when operated in symmetrical and unsymmetrical modes of operation, respectively.

The work is well thought-out as follows. The operation circuit of the proposed nine-level basic structure is elaborated in Section 2. The determination of the capacitor rating for the proposed converter has been discussed in Section 3. Sections 4 and 5 assert the cascaded connection and comparative analysis. Sections 6 and 7 propound the loss estimation of the proposed 9L-SCMLI and performance analysis of 9L AND 17L-SCMLIs using simulation results and experiment results of 9L-SCMLI at different loading conditions.

2 | CIRCUIT DESCRIPTION OF THE PROPOSED 9L-SCMLI

Figure 1 shows the basic structure of the nine-level Switched-Capacitor Multilevel Inverter (9L-SCMLI) used for synthesizing a nine-level output waveform. The basic 9L-SCMLI structure is modeled using eight unidirectional switches, one bidirectional switch (S_7), two diodes, two capacitors, and a single input DC source. The switches S_1, S_2, and S_9, S_{10} are the switching devices of a half-bridge circuit. The capacitors C_1 and C_2 can be connected either in series or in parallel through the S_3, S_4, S_5, and S_6, and diodes D_1 and D_2 for voltage addition, and capacitor charging. The input DC source, along with two capacitors C_1 and C_2 and switching devices, is used to synthesize different voltage levels. The blocking voltage value of the switches S_1–S_4 and S_8–S_9 is V_{dc}, whereas for the switches S_5–S_6, it is $2V_{dc}$. The switch S_7 requires to block a voltage of $0.5V_{dc}$, which ultimately reduces the cost of the switch S_7 employed. The gate pulses for the 9L-SCMLI switches are generated by using the level shift pulse width modulation technique. The conduction path during each level of the output voltages is shown in Figures 2 and 3. The operations of each level for the nine-level outputs are analyzed separately, and the corresponding switching operations and the voltage levels are given in Table 1.

Figure 2a–e illustrates the current conduction path for the proposed 9L-SCMLI during the zero and positive levels of the voltage generation. For zero level, the switches S_2, S_3, S_4, and S_9 are turned ON, as shown in Figure 2a. Here, the capacitors C_1 and C_2 are charged to the potential of $V_{dc}/2$ through switches S_3 and S_4 and diodes D_1 and D_2. Based on Figure 2b, the switches S_2, S_3, S_4, and S_7 are turned ON to obtain the first level of the positive voltage $V_{dc}/2$, which is

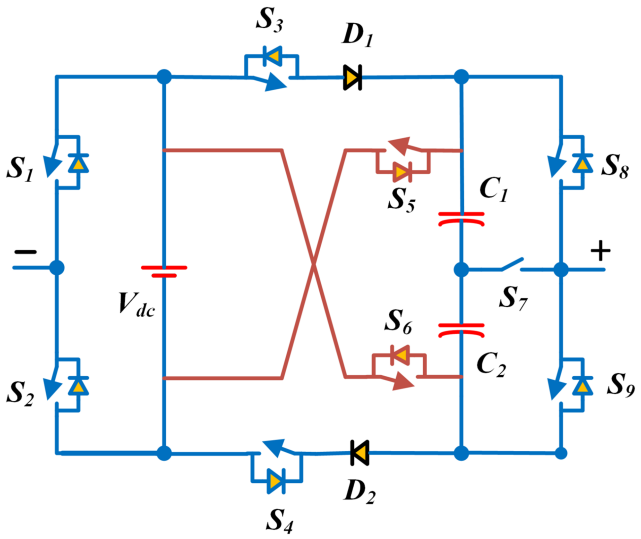


FIGURE 1 Proposed basic structure of 9L-SCMLI [Colour figure can be viewed at wileyonlinelibrary.com]

obtained from the terminals of the capacitor C_2. In the meantime, the capacitor C_1 is charged from the voltage source through switches S_3 and S_4 and diodes D_1 and D_2. The second positive level $+V_{dc}$ is created without involving any of the capacitors by turning ON the switches S_2, S_3, S_4, and S_8, as shown in Figure 2c. The capacitors C_1 and C_2 are charged during this cycle also, as mentioned in the path at level zero and level $V_{dc}/2$ of generation. For Figure 2d, the switches S_2, S_6, and S_7 are turned ON to synthesize the third positive level voltage $+3V_{dc}/2$, by adding the capacitor voltage C_1 and the source voltage.

The voltage across the capacitors C_1 and C_2 and the source voltage V_{dc} is added by turning ON the switches S_2, S_6, and S_8 to generate fourth positive level voltage $+2V_{dc}$ as shown in Figure 2e. The first negative level of current flow has been illustrated in Figure 3a, the switches S_1, S_3, S_4, and S_7 are turned ON to obtain the first level negative voltage $-V_{dc}/2$. The bidirectional switch S_7 proves to be effective in blocking the positive and negative voltages during the first levels. The output voltage level $-V_{dc}$ can be traced out by the switches highlighted as depicted in Figure 3b. Here, the input source voltage is connected directly across the load. In the same period, the capacitors have charged to the required voltage level. The input DC source is a series connected with capacitor C_1 to synthesize the voltage level $(-3V_{dc}/2)$ and the conduction path where the switches S_1, S_5, and S_7 are turned ON as shown in Figure 3c. At the last stage, the capacitors C_1 and C_2 are connected in series with the input DC source to apply $(-2V_{dc})$ voltage across the load is shown in Figure 3d. Here, the switches S_1, S_5, and S_8 are turned ON to achieve the fourth negative level.

Table 1 shows the conducting switches, capacitor states, and the corresponding step angle in the various levels of output voltage generation, where "1" denotes the ON state & "0" denotes the OFF state of the switches. The step angle is shown only for the quarter cycle of the output waveform, and it is used at the time of determination of capacitance value. The number of switches in conduction at different levels is not more than 6, and the switch pairs (S_1 & S_2 and S_8 & S_9) are complementary switches either one of them will be in conduction mode or both will be in the off state.

It is clear from Table 1 that both capacitors are equally charged and discharged to the voltage level of $V_{dc}/2$ for the same period during one full cycle of the output voltage waveform. The above phenomenon avoids the need for additional charge balancing circuits and sensors, thereby reducing the overall cost of the system. The system can boost deliver a terminal voltage which is twice the input voltage. The maximum peak inverse voltage (PIV) for the switches S_5 and S_6 is $2V_{dc}$ and V_{dc} for the switches S_1, S_2, S_3, and S_4, but the switch S_7 has to withstand half of the input voltage only. The total standing voltage of the proposed topology is determined as $11V_{dc}$, which is approximately half the value of the topology presented in previous study.[29]

3 | DETERMINATION OF CAPACITANCE

The longest discharging cycle has been estimated using Figure 4 to calculate the farad value of the capacitors to be used in the 9L-SCMLI topology. The longest discharging cycle for capacitor C_1 and C_2 occurs during the negative and

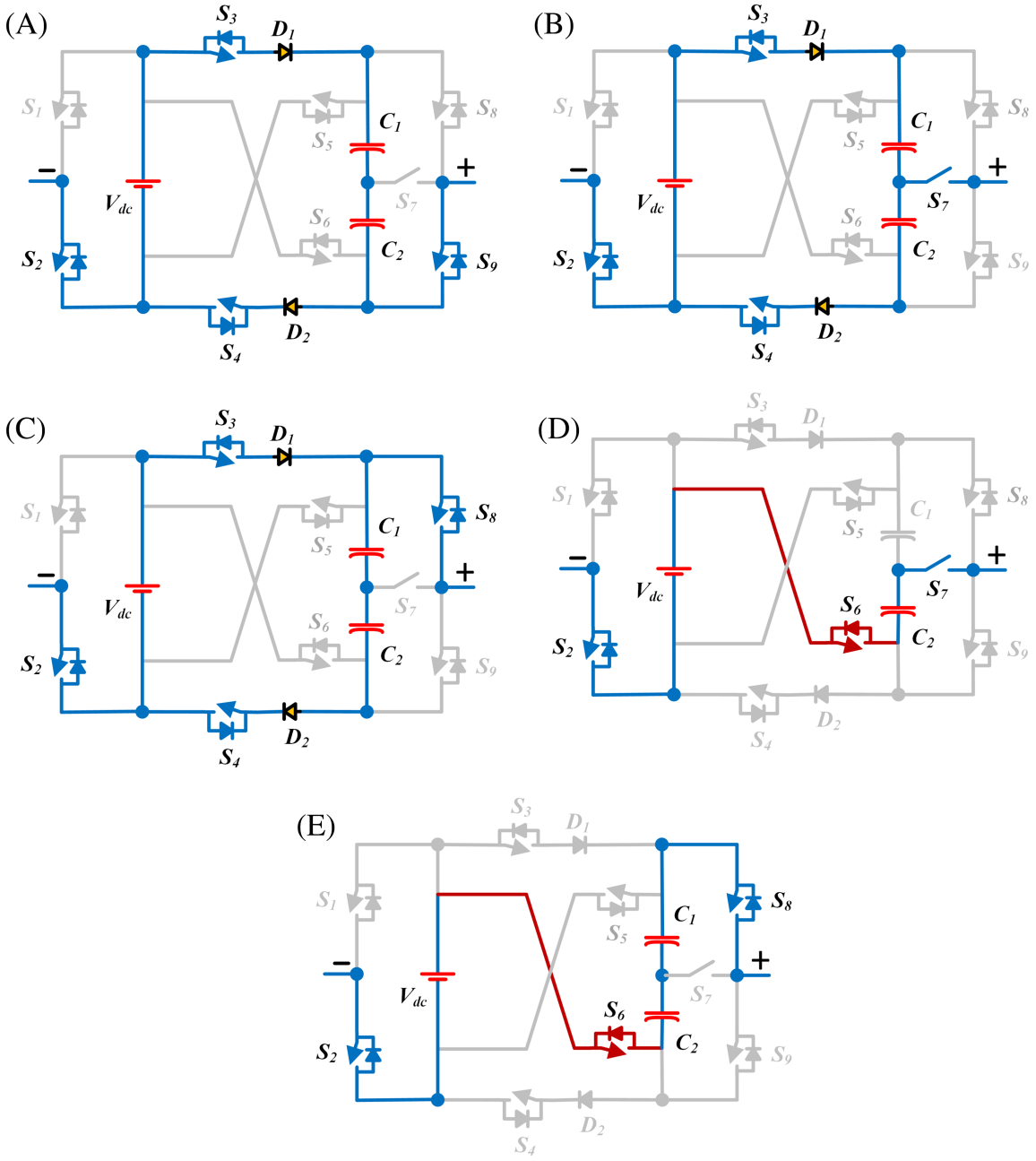


FIGURE 2 Current flowing paths at zero and positive levels: (a) zero, (b) first positive $V_{dc}/2$, (c) second positive V_{dc}, (d) third positive $3V_{dc}/2$, (e) fourth positive $2V_{dc}$ [Colour figure can be viewed at wileyonlinelibrary.com]

positive half-cycle, respectively, for the equal time interval. The capacitor ripple voltage has been kept at 10% of the input voltage, and the following Equations 1–7 have been used to determine the capacitance value.

A suitable specification has been chosen for the capacitances C_1 and C_2 based on their most extended discharging cycle.[16] The duration of each steps of the staircase output waveform has been given in Table 2.

Here, T_s is the time period of the output voltage and is obtained from output voltage frequency. From Figure 4, the longest discharging cycle of the capacitor C_1 happens during the time interval of α_{10}–α_{13}, whereas for the capacitor C_2 occurs at α_3–α_7 even though the capacitor discharges at various intervals in both positive and negative cycles of the fundamental frequency. The charge in the capacitor C_1 and C_2 during the time period of α_{11}–α_{15} & α_3–α_7 can be written as in Equations 1 and 2

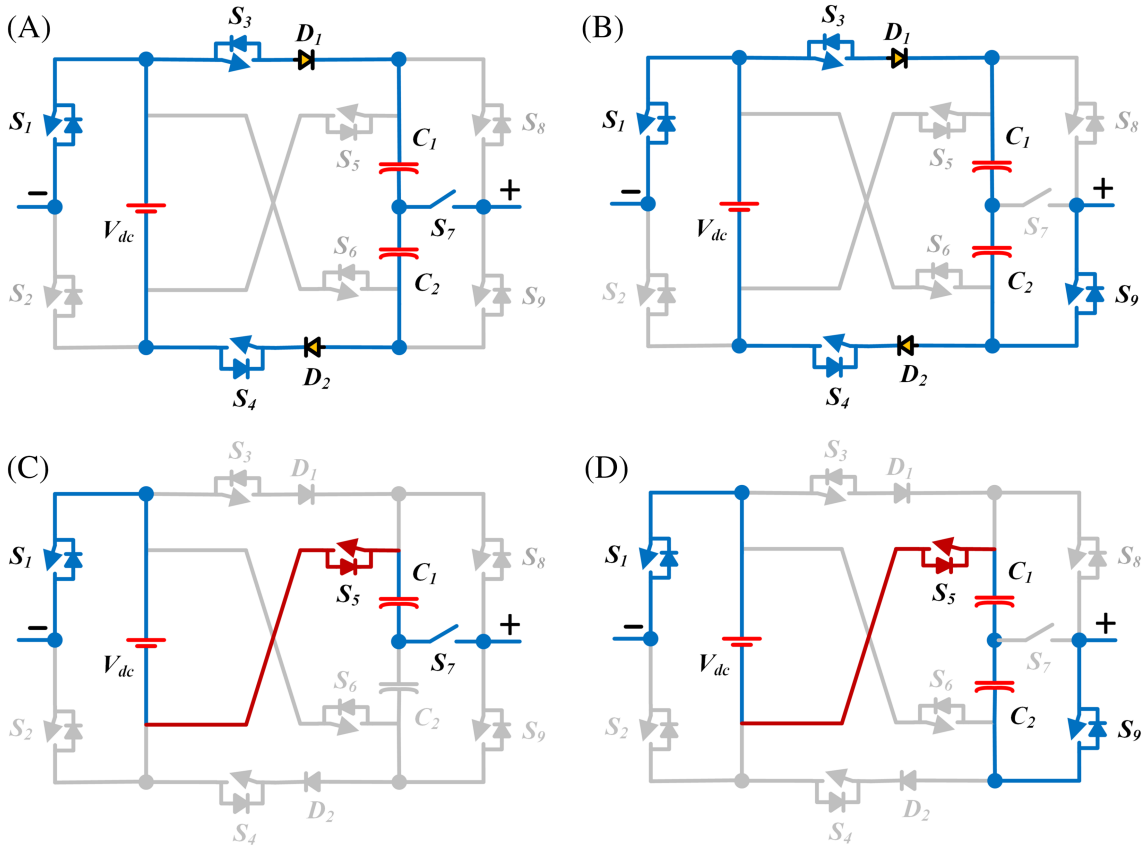


FIGURE 3 Current flowing paths at different negative levels: (a) first negative $-V_{dc}/2$, (b) second negative $-V_{dc}$, (c) third negative $-3V_{dc}/2$, (d) fourth negative $-2V_{dc}$ [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1 Switching states of proposed 9L-SCMLI topology

Switches/voltage levels	$+2V_{dc}$	$+3V_{dc}/2$	$+V_{dc}$	$+V_{dc}/2$	0	$-V_{dc}/2$	$-V_{dc}$	$-3V_{dc}/2$	$-2V_{dc}$
S_1	0	0	0	0	0	1	1	1	1
S_2	1	1	1	1	1	0	0	0	0
S_3	0	0	1	1	1	1	1	0	0
S_4	0	0	1	1	1	1	1	0	0
S_5	0	0	0	0	0	0	0	1	1
S_6	1	1	0	0	0	0	0	0	0
S_7	0	1	0	1	0	1	0	1	0
S_8	1	0	1	0	0	0	0	0	0
S_9	0	0	0	0	1	0	1	0	1
D_1	0	0	1	1	1	1	1	0	0
D_2	0	0	1	1	1	1	1	0	0
C_1	D	NC	C	C	C	C	C	D	D
C_2	D	D	C	C	C	C	C	NC	D

Abbreviations: C, charging; D, discharging; NC, no change.

$$Q_{c1} = \int_{\propto_{12}}^{\propto_{16}} I_L(t)\, dt$$

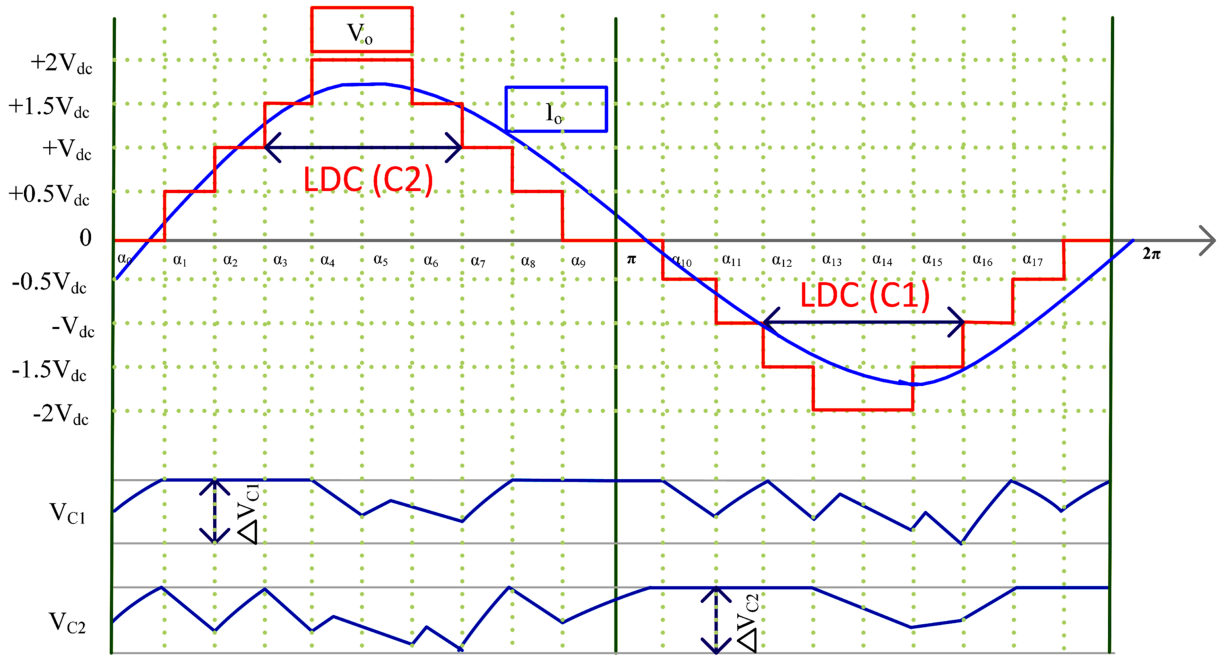


FIGURE 4 Nine level staircase output voltage, current and the capacitors waveform [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 2 Step angle calculation for staircase output waveform

Step angle (α)	α_0	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8
Time period (S)	0	$T_s/20$	$T_s/10$	$3T_s/20$	$T_s/5$	$T_s/4$	$3T_s/10$	$7T_s/20$	$2T_s/5$
Step angle (α)	α_9	α_{10}	α_{11}	α_{12}	α_{13}	α_{14}	α_{15}	α_{16}	α_{17}
Time period (S)	$9T_s/20$	$6T_s/10$	$13T_s/20$	$7T_s/10$	$3T_s/4$	$4T_s/5$	$17T_s/20$	$9T_s/10$	$19T_s/20$

$$Q_{c2} = \int_{\propto_3}^{\propto_7} I_L(t)\, dt$$

Here, $I_L(t)$ is the amplitude of the load current. For an R-L load, the instantaneous value of load current can be estimated by using (2)

$$I_L(t) = I_m Sin(\omega T - \varphi)$$

By substituting Equation 3 in Equations 1 and 2, we get the simplified equation as follows:

$$Q_{c1} \geq \frac{I_m}{\omega}\left[Cos\left(\frac{7\pi}{5} - \varphi\right) - Cos\left(\frac{9\pi}{5} - \varphi\right)\right]$$

$$Q_{c2} \geq \frac{I_m}{\omega}\left[Cos\left(\frac{3\pi}{10} - \varphi\right) - Cos\left(\frac{7\pi}{10} - \varphi\right)\right]$$

The optimum value for capacitor $C_{1,2}$ can be calculated as follows

$$C_{Opt,1} \geq \frac{I_m}{\omega \times k \times V_{dc}} \left[Cos\left(\frac{7\pi}{5} - \varphi\right) - Cos\left(\frac{9\pi}{5} - \varphi\right) \right]$$

$$C_{Opt,2} \geq \frac{I_m}{\omega \times k \times V_{dc}} \left[Cos\left(\frac{3\pi}{10} - \varphi\right) - Cos\left(\frac{7\pi}{10} - \varphi\right) \right]$$

4 | CASCADED STRUCTURE OF 9L-SCMLI

The proposed topology is cascaded to synthesize a higher level of output voltage, as shown in Figure 5. On cascading, the circuit operates in both symmetrical and unsymmetrical modes of operation. In symmetrical mode, the input voltage of the cascaded module is equal to the basic module; during the unsymmetrical mode of operation, the input voltage of the cascaded modules is different from the basic counterpart. The maximum output voltage level that can be synthesized during the symmetrical mode of operation is 17 levels.

During the unsymmetrical mode of operation, the two input voltage sources of the extended topology can be set in binary and trinary patterns; the system will be able to generate 25 and 33 output voltage levels. The maximum voltage level that can be generated during the unsymmetrical mode of operation is 49 by keeping two input voltages as multiples of 5, for example, V_{dc} and $5V_{dc}$, respectively. The boosting factor during the symmetrical and unsymmetrical mode of operation is also two, but the number of levels is increased apparently, which leads to a decrease in THD value, and it is evident from Figure 5h. During cascaded operation, the flying capacitors in all modules are charged to the potential equal to half of the source voltage.

If N is the number of cascaded modules connected horizontally to the basic topology to intensify the number of levels generated, the number of output voltage levels (N_{Level}) obtained in the form staircase waveform by means of cascading is expressed in Equation 8.

$$N_{Level} = 8N + 1$$

The components involved like IGBTs ($N_{switches}$), Drivers ($N_{Drivers}$), Diodes (N_{Diodes}), and Capacitors ($N_{Capacitors}$) required for synthesizing N_{level} can be determined by equation (9–11).

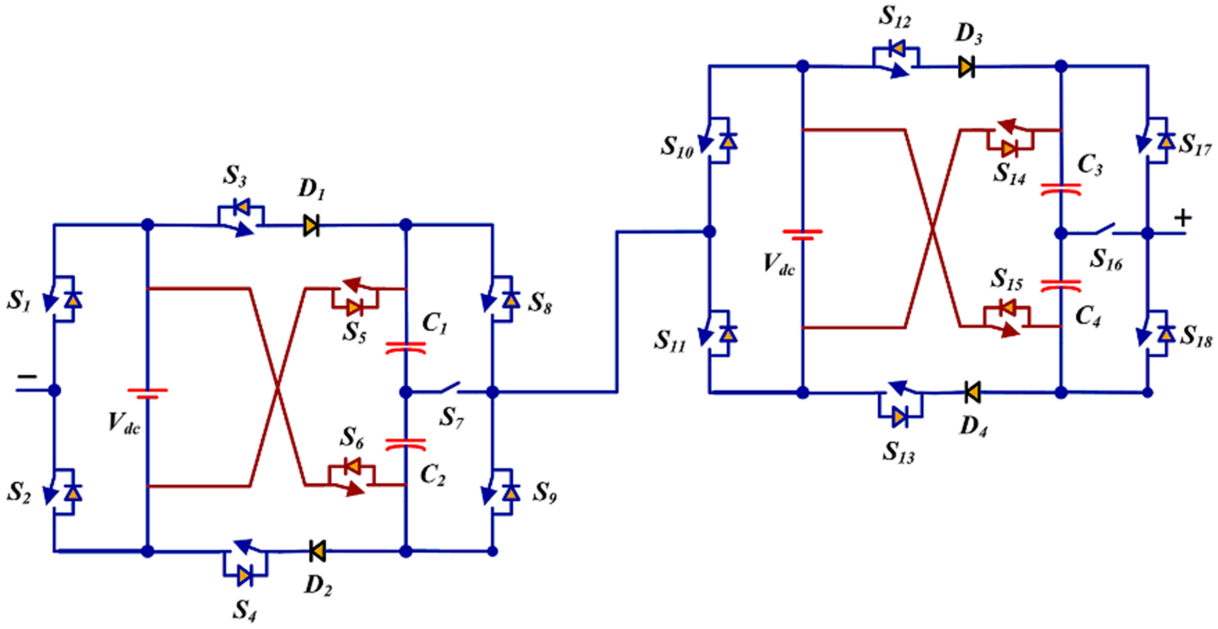


FIGURE 5 Cascaded model of the proposed 9L-SCMLI converter [Colour figure can be viewed at wileyonlinelibrary.com]

$$N_{Switches} = 10\,\mathrm{N}$$

$$N_{Drivers} = 9N$$

$$N_{Diodes} = N_{Capacitors} = 2N$$

The maximum number of levels and maximum output voltage can be generated by operating the inverter in symmetrical and asymmetrical modes. The number of levels and output voltage can be determined by using Equations 12–15.

Table 3 illustrates the capacitor connections for the corresponding switching sequences. The respective output voltages have been measured from the output terminals and depicted in Table 3.

$$N_{level,sym} = 8N + 1$$

$$V_{o,Sym} = 2N\,V_{dc}$$

$$N_{level,asym} = 2 \times \left(5^N - 1\right)\ N \geq 2$$

$$V_{o,Asym} = \left(5^N - 1\right)V_{dc}$$

where N is the number of cascaded modules.

5 | COMPARISON OF PROPOSED TOPOLOGY WITH EXISTING MLIs

Table 4 compares the various converter models in the literature with the proposed converter. The essential parameters for the comparison with the different models include the number of levels, number of DC sources, IGBTs, Diodes, Capacitors, Driver circuits, boosted voltage value, the total standing voltage of the switches, extended ability, and the way to obtain negative levels.

TABLE 3 Switching sequences for the capacitor connections and the corresponding output voltages in cascaded connection

No. of levels	ON switches							C_1	C_2	C_3	C_4	V_0
1.	S_2	S_6	S_8	S_{11}	S_{15}	S_{17}	-	D	D	D	D	$4V_{dc}$
2.	S_2	S_6	S_8	S_{11}	S_{15}	S_{16}	-	D	D	N	D	$3.5V_{dc}$
3.	S_2	S_6	S_8	S_{11}	S_{12}	S_{13}	S_{17}	D	D	C	C	$3V_{dc}$
4.	S_2	S_6	S_8	S_{11}	S_{12}	S_{13}	S_{16}	D	C	N	C	$2.5V_{dc}$
5.	S_2	S_6	S_8	S_{11}	S_{13}	S_{18}	-	C	C	C	C	$2V_{dc}$
6.	S_2	S_6	S_7	S_{11}	S_{13}	S_{18}	-	C	C	C	D	$1.5V_{dc}$
7.	S_3	S_4	S_8	S_{11}	S_{13}	S_{18}	S_2	C	C	C	C	V_{dc}
8.	S_3	S_4	S_7	S_{11}	S_{13}	S_{18}	S_2	D	C	C	C	$0.5V_{dc}$
9.	S_1	S_3	S_8	S_{10}	S_{12}	S_{17}	-	C	C	C	C	0
10.	S_1	S_3	S_4	S_7	S_{10}	S_{12}	S_{17}	D	C	C	C	$-0.5V_{dc}$
11.	S_1	S_3	S_4	S_9	S_{10}	S_{12}	S_{17}	C	C	C	C	$-V_{dc}$
12.	S_1	S_5	S_7	S_{10}	S_{12}	S_{17}	-	C	C	D	C	$-1.5V_{dc}$
13.	S_1	S_5	S_9	S_{10}	S_{12}	S_{17}	-	C	C	C	C	$-2V_{dc}$
14.	S_1	S_5	S_9	S_{10}	S_{12}	S_{13}	S_{16}	N	D	C	C	$-2.5V_{dc}$
15.	S_1	S_5	S_9	S_{10}	S_{12}	S_{13}	S_{18}	D	D	C	C	$-3V_{dc}$
16.	S_1	S_5	S_9	S_{10}	S_{14}	S_{16}	-	N	D	D	D	$-3.5V_{dc}$
17.	S_1	S_5	S_9	S_{10}	S_{14}	S_{18}	-	D	D	D	D	$-4V_{dc}$

TABLE 4 Comparison of proposed 9S-SCMLI converter with various other topologies

Topology	N_{Levels}	$N_{Sources}$	N_{IGBTs}	N_{Diodes}	$N_{Capacitors}$	$N_{Drivers}$	Voltage boost	TSV	Extended ability	Negative level
Hinago[30]	7	1	10	0	3	10	3	16	No	H bridge
Junzeng[12]	9	1	9	2	2	9	2	15	No	H bridge
J. Liu[13]	9	2	12	2	2	12	2	22	Yes	H bridge
J. S. Ali[11]	9	1	11	1	2	10	2	11	Yes	In built
Reza[28]	9	1	10	1	2	10	2	24	Yes	In built
Lee[29]	9	1	12	0	2	10	2	11	No	In built
Saeedian[21]	9	1	8	1	4	8	2	16	Yes	H bridge
Amir[4]	9	1	19	1	3	19	2	19	Yes	H bridge
Proposed	9	1	10	2	2	9	2	11	Yes	In built

The proposed topology is compared mainly with topologies having a single DC source except for topology in the literature.[13] Figure 6a shows the comparison chart of the number of IGBTs used in the proposed topology and topologies in previous works[4,11,28] for synthesizing various levels of the output waveform, and it is visible that the proposed topology requires fewer components than its counterparts. Figure 6b indicates that the number of capacitors necessary for the proposed topology is less as compared with topologies in the literature.[4,21] The standing voltage of the switches is the vital parameter to be considered because it has a direct impact on the cost of MLI. As seen from the Figure 6c, the total standing voltage (TSV) value from previous works[12,13,26,30] are more than the proposed topology. From the aforementioned analysis, it is observed that the proposed converter delivers better output voltage with reduced circuit components and cost when compared with other topologies.

6 | POWER LOSS AND EFFICIENCY

In this section, the theoretical calculation of power loss estimation is being discussed, and the derived equations are used to calculate the efficiency of the proposed 9L-SCMLI. Here, conduction loss and switching loss for each of the IGBT switches and diodes used in the 9L-SCMLI system are estimated separately.

6.1 | Conduction losses

In multilevel inverters, the IGBT switches are turned on sequentially to synthesize voltage levels leads to conduction loss. The proposed topology consists of two half-bridge units constituted by switches (S_1, S_2, S_8, and S_9), capacitor charging switches (S_3, S_4, D_1, and D_2), complementary switches (S_5 and S_6), and the bidirectional switch S_7. Here, the power loss occurring in each of the IGBT switches is estimated separately for calculating total conduction loss.

Half-bridge unit 1, comprises of switches S_1 and S_2, among that either one will be in load current path for half the period of the fundamental cycle. Therefore, the average conduction loss for the switch S_1, which is in conduction for half the period of the fundamental cycle is obtained by the below equation:

$$P_{Con,H} = \frac{1}{2\pi}\int_0^{\pi} I_L^2(t) R_{on,T}.dt$$

The load current through the switches is assumed to be sinusoidal, and the load current in the above equation can be rewritten as in Equation 17

$$I_L(t) = I_m \sin(wt)$$

where I_m is the maximum current flowing through the switch.

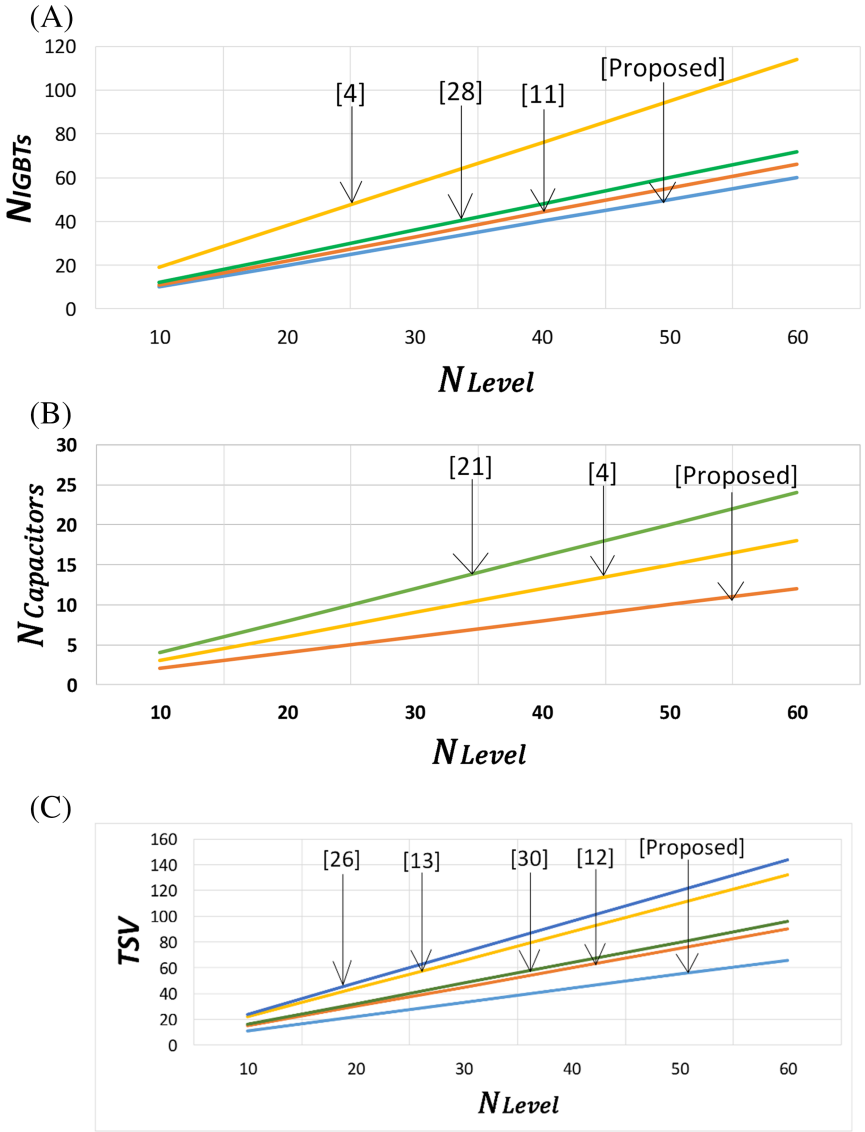


FIGURE 6 Comparison of (a) number of levels versus number of IGBTs (b) number of levels versus number of capacitors (c) number of levels versus Total standing voltage [Colour figure can be viewed at wileyonlinelibrary.com]

$$P_{Con,H(1)} = \frac{1}{2\pi}\int_0^{\pi} I_m^2 \, sin^2(wt) R_{on,T} \, dt$$

Equation 18 can also be used for estimating conduction loss in the switch S_2.
Similarly, the average conduction loss in the half-bridge unit 2 constituted by S_8 and S_9 is given in Equation 19

$$P_{Con,H(2)} = \frac{1}{\pi}\left[\int_0^{t_1} 0 \, R_{on,T} \, dt + \int_{t_1}^{t_2} I_m^2 \, sin^2(wt) R_{on,T} \, dt + \int_{t_2}^{t_3} 0 \, R_{on,T} \, dt + \int_{t_3}^{t_4} I_m^2 \, sin^2(wt) R_{on,T} \, dt\right]$$

A similar procedure is used for calculating the conduction loss of other switches. The total conduction loss in capacitor charging switches and diodes ($P^T_{Con,C}$), complementary switches ($P^T_{Con,Com}$), and bidirectional switches ($P^T_{Con,B}$) is given by Equations 20–22.

$$P^{T}{}_{Con,C} = \frac{1}{\pi}\left[\int_{0}^{t_2} I_m^2\ sin^2(wt)(R_{on,T} + R_{on,D})dt + \frac{1}{\pi}\int_{t_2}^{t_4} 0\,(R_{on,T} + R_{on,D})\,dt\right]$$

$$P^{T}{}_{Con,Com} = \frac{1}{\pi}\left[\int_{0}^{t_3} 0\,R_{on,T}\,dt + \int_{t_3}^{t_4} I_m^2\ sin^2(wt)R_{on,T}\,dt\right]$$

$$P^{T}{}_{Con,B} = \frac{2}{\pi}\left[\int_{0}^{t_3} 0\,R_{on,T}\,dt + \int_{t_3}^{t_4} I_m^2\ sin^2(wt)R_{on,T}\,dt\right]$$

Here, $R_{on,T}$ & $R_{on,D}$ are the IGBT and diode on state resistance, respectively. Therefore, the total conduction loss (P_{Con}^{T}) of the proposed 9L-SCMLI during the full cycle of the output voltage waveform can be calculated using Equation 23.

$$P_{Con}^{T} = P^{T}{}_{Con,H} + P^{T}{}_{Con,C} + P^{T}{}_{Con,Com} + P^{T}{}_{Con,B}$$

6.2 | Switching losses

The switching loss in IGBT happens due to overlapping of voltage and current during the transition phenomenon, that is, turn on to turn off or vice versa.[24] The switching loss during turn on & turn off period of the IGBT switches are obtained by Equations 24 and 25 respectively.

$$P_{SW,On} = \frac{1}{6} fIV_{ON}\,t_{ON}$$

where V_{ON} is the voltage drop across the switch; when it is ON, this will happen due to the parasitic capacitance resistance of the switch. The current flowing through the IGBT switch during conduction is I_C, which will vary based on the voltage level in which the switch is turned ON. The time taken for the IGBT to turn ON is t_{ON}. Similarly, from the linearized switching model, during turn OFF, the switching loss can be obtained by calculating the power dissipated in a switch

$$P_{SW,Off} = \frac{1}{6} fIV_{OFF}\,t_{OFF}$$

where V_{OFF}, I_{OFF}, t_{OFF} are IGBT open circuit voltage, current flowing through IGBT before turning off and turn off time, respectively.

The Equations 24 and 25 are used to calculate average switching loss in each of the switches. For the switches S_1 & S_2 in half-bridge unit 1, it has only one turn on for a full period of the fundamental cycle. In this scenario, the switching loss of the $P_{SW,S1}$ is given by Equation 26

$$P_{SW,H1} = \frac{1}{6} fIV_{ON}\,t_{on}$$

A similar procedure can be used to derive an equation for other switches also. The total switching loss for the proposed topology has been calculated by using Equation 27

$$P_{Sw}^{T} = \sum\nolimits_{i=1}^{12} P_{Si}$$

6.3 | Capacitor ripple loss

The power loss in the capacitor happens due to ripple voltage available across each of the capacitors. The ripple voltage is estimated by calculating the longest discharging time of the capacitor. If I_{ci} is the current through the capacitor "i," and C_i is the capacitance pertain to the capacitor "i," then the voltage ripple can be estimated by using Equation 28.

$$\Delta V_{c,i} = \frac{1}{2\pi f C_i}\int_{t_m}^{t_n} I_{ci}(t)dt \quad i = 1,2$$

where t_m & t_n are the start time and end time in the longest discharging cycle of the capacitor, and for the proposed 9L-SCMLI, it can be obtained from Figure 4.

The voltage ripple across the capacitors can be estimated using an expression as given in Equations 29 and 30

$$\Delta V_{c,1} = \frac{I_m}{2\pi f C_1}\left[Cos\left(\frac{7\pi}{5} - \varphi\right) - Cos\left(\frac{9\pi}{5} - \varphi\right)\right]$$

$$\Delta V_{c,2} = \frac{I_m}{2\pi f C_1}\left[Cos\left(\frac{3\pi}{10} - \varphi\right) - Cos\left(\frac{7\pi}{10} - \varphi\right)\right]$$

By estimating voltage ripple losses incurred in the capacitors C_1 and C_2, the total ripple loss of the system has been evaluated by using Equation 31

$$P_{Rip}^{T} = \frac{1}{2\pi}\sum_{i=1}^{2} C_i \Delta V_{Ci}^2$$

The total losses and efficiency can be obtained by using the expression in Equation 32 and Equation 33, respectively.

$$P_{Loss} = P_{Con}^{T} + P_{SW}^{T} + P_{Rip}^{T}$$

$$\eta = \frac{P_{out}}{P_{in} + P_{Loss}}$$

7 | SIMULATION AND EXPERIMENTAL RESULTS

A simulation platform is created using MATLAB/SIMULINK to evaluate the performance and check the feasibility of proposed 9L-SCMLI. Design parameters of the 9L-SCMLI used in simulation and experimental environment are shown in Table 5. The level-shifted PWM technique is employed for generating gate pulse to turn ON & OFF the 9L-SCMLI IGBT switches to synthesize output voltage nearer to the sinusoidal waveform. In this modulation technique, for the proposed inverter to generate $8N + 1$ level, a $8N$ triangular carrier waveform is needed with the same frequency. The sinusoidal waveform with the same frequency as that of the required output voltage frequency can be used as a modulating signal. The carrier wave and reference wave are compared with generate gate pulse and switches are turned

TABLE 5 Simulation and experimental parameters

Descriptions	Simulation	Experimental prototype
Input DC	100 V	100 V
Capacitor rating	50V/4700 μF	50V/4700 μF
R-L load	R = 50 ohms, L = 100 mH	R = 50 ohms, L = 50 mH
Fundamental/switching frequency	50 Hz/5 KHz	50 Hz/5 KHz

on. In this section, the simulation and experimental results of the proposed 9L-SCMLI and simulation results of 17L-SCMLI are discussed in detail.

The output voltage and current waveforms of 9L-SCMLI for a fixed load of R = 50 Ω and R = 50 Ω L = 100 mH is shown in Figure 7a,b. The output voltage waveform shows that the maximum voltage is 200 V, which is twice the input voltage, thus confirming the boosting ability of the proposed topology. From the load current waveform, it can be viewed that the load current is 4A for R load and 2.5 A for RL load. The change in load from R to RL is performed and the current waveform in Figure 7c confirms the stability of the proposed converter by responding within a cycle of the operation. The 17L-SCMLI is simulated and the corresponding results are shown in Figure 7e–h. The output voltage and current waveforms of 17L-SCMLI for fixed and dynamic load values are shown in Figure 7e–g here, and the input voltage of both modules is fixed as 100 V, and in this case, also the output voltage has the boosting factor of 200%. The total harmonic distortion value of both 9L & 17L-SCMLI is perceived as 15.63% and 7.82%, respectively, which is depicted in Figure 7d,h. Owing to an increase in the number of levels or steps, the 17L-SCMLI has better THD value as compared with 9L-SCMLI. The decrease in THD value reduces the filtering components size and the cost.

Figure 8a,b shows the voltage and current waveform of the two involved capacitors C_1 and C_2 of 9L-SCMLI. As the input voltage is 100 V, the capacitor voltages are clamped to half of the input voltage. It is also observed that both the capacitors are capable of settling down quickly to the change in load operation, providing better stability to the system. Figure 8b shows the current through the flying capacitors C_1 and C_2, and it is seen that the capacitor's current is slightly higher than the load current and it is free from current sag and swell during charging and discharging periods of the operation.

The voltage and current of the switch S_1 under the RL load condition are shown in Figure 9a,b, respectively. It was observed from Figure 9a that voltage across the switch is 100 V, which is equal to the input voltage. From Figure 9b, it is evident that the peak current through the switch is equal to the load current.

To validate the performance of 9L-SCMLI, the experimental prototype was fabricated with values as specified in Table 5. Figure 10 illustrates the experimental setup comprising 9L-SCMLI with gate driver circuits, FPGA controller,

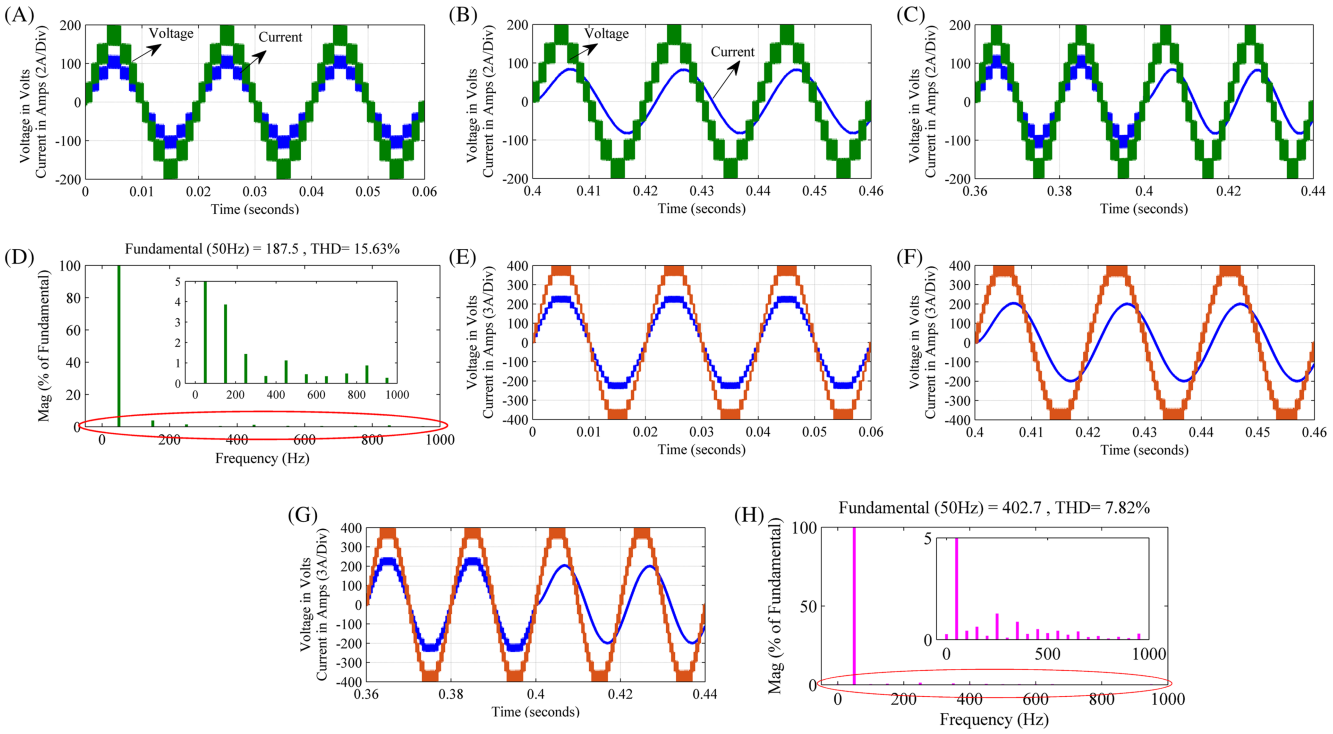


FIGURE 7 Simulated waveforms of 9L-SCMLI & 17L-SCMLI: 9L-SCMLI (a) output voltage and current for R = 50 Ω, (b) output voltage and current for R = 50 Ω, L = 100 mH, (c) output voltage and current for change in load R = 50 Ω to R = 50 Ω, L = 100 mH, (d) voltage THD, 17L-SCMLI (e) output voltage and current for R = 50 Ω, (f) output voltage and current for R = 50 Ω, L = 100 mH, (g) output voltage and current for change in load R = 50 Ω to R = 50 Ω, L = 100 mH, (h) voltage THD [Colour figure can be viewed at wileyonlinelibrary.com]

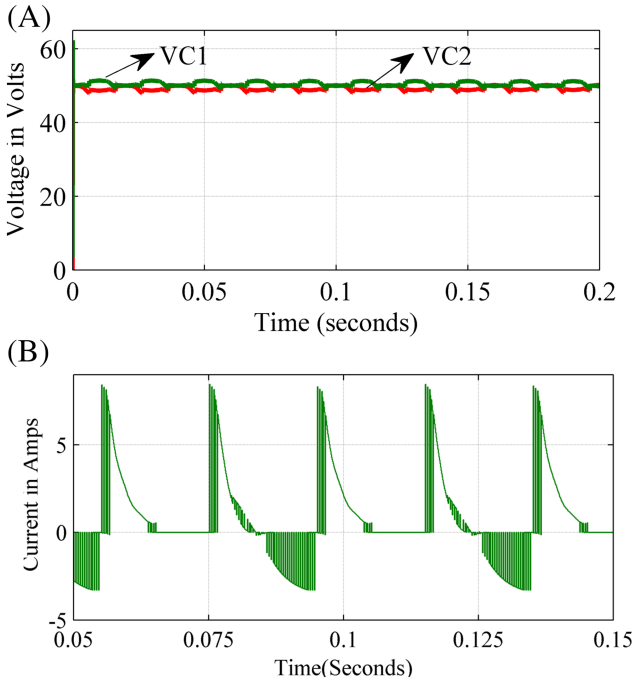


FIGURE 8 (a) Simulated voltage waveforms across the capacitors C_1 and C_2 (b) simulated current waveform through the capacitors [Colour figure can be viewed at wileyonlinelibrary.com]

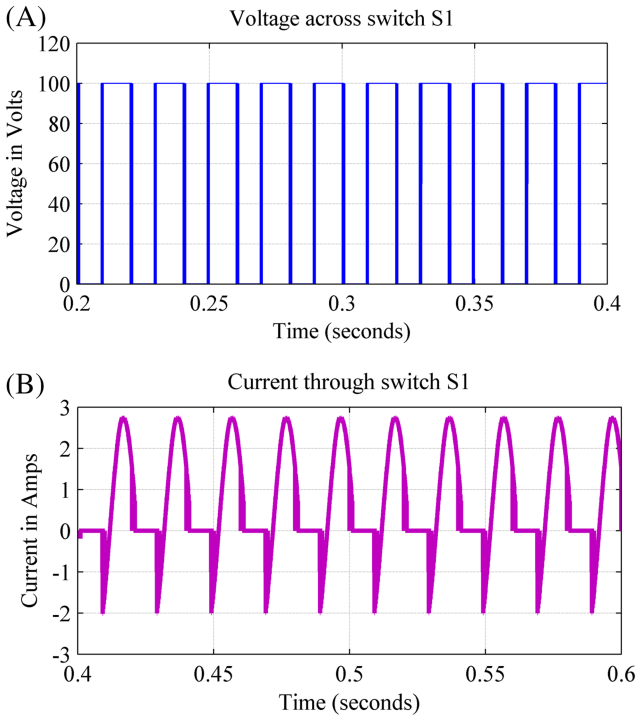


FIGURE 9 (a) Simulated voltage waveform across the switch S_1 (b) simulated current waveform through the switch S_1 [Colour figure can be viewed at wileyonlinelibrary.com]

input Dc voltage source, DSO, and RL load. The IGBT employed in the experimental prototype is Semikron IGBT switches (SKM75GB063D) having on-state resistance of 14mΩ and the diode is 25 HMR with an internal resistance of 3mΩ. The effectiveness of the proposed topology is validated in high-frequency modulation. In high-frequency modulation, the FPGA controller was operated at 5 kHz frequency, and the output voltage waveform in Figure 9 indicates different commutation occurring at each of the levels.

The waveform shown in Figure 11 shows the generated nine-level staircase-output voltages with the magnitude of each level equal to half of the input voltage. It is observed that the maximum output voltage is twice the input voltage indicating the boosting ability of the proposed inverter. The output voltage and load current are represented in staircase

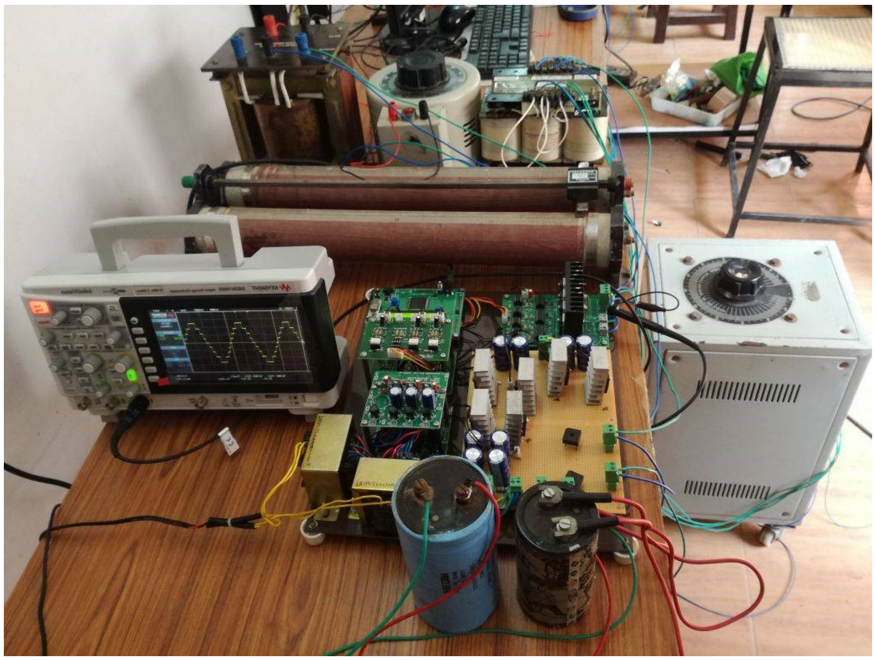


FIGURE 10 Prototype model of 9L-SCMLI [Colour figure can be viewed at wileyonlinelibrary.com]

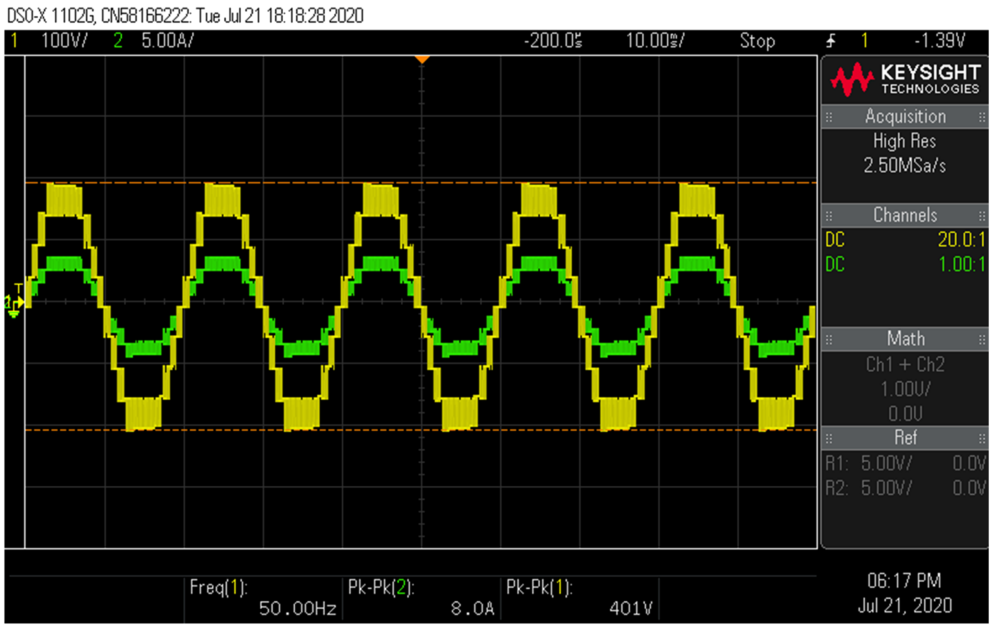


FIGURE 11 Experimental output voltage and current waveform for R = 50 Ω [Colour figure can be viewed at wileyonlinelibrary.com]

waveform when connected to "R" load which can be observed from Figure 10 and the peak current value observed from the waveform is 4 A for the load value of R = 50 Ω.

Figure 12 shows the experimental output voltage and current waveform fed with RL load. For the load value of R = 50 Ω and L = 50 mH, the peak-peak load current is found to be 6.6 A. The stepped current waveform traced out during resistive load condition is smoothened because of the addition of inductance complies with its natural property to filter out the ripples can be seen from the Figure 10.

The load change is performed to evaluate the dynamic behavior of the proposed topology, and it shows better adoption to the varying conditions. Here, the load value is changed from R = 50 Ω to R = 50 Ω, L = 50 mH, and the model

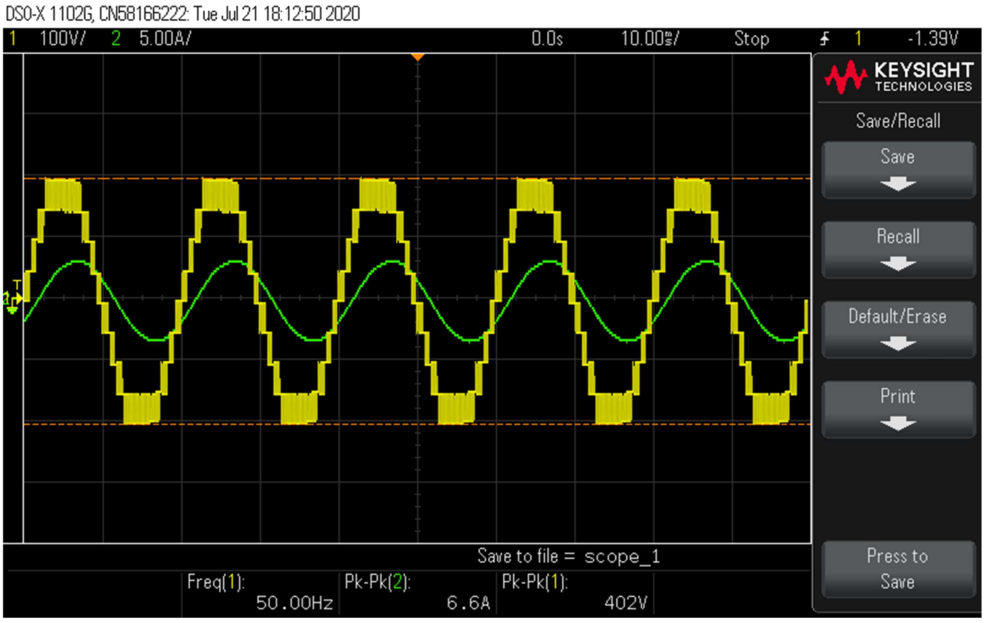


FIGURE 12 Experimental output voltage and current waveform for R = 50 Ω L = 50 mH [Colour figure can be viewed at wileyonlinelibrary.com]

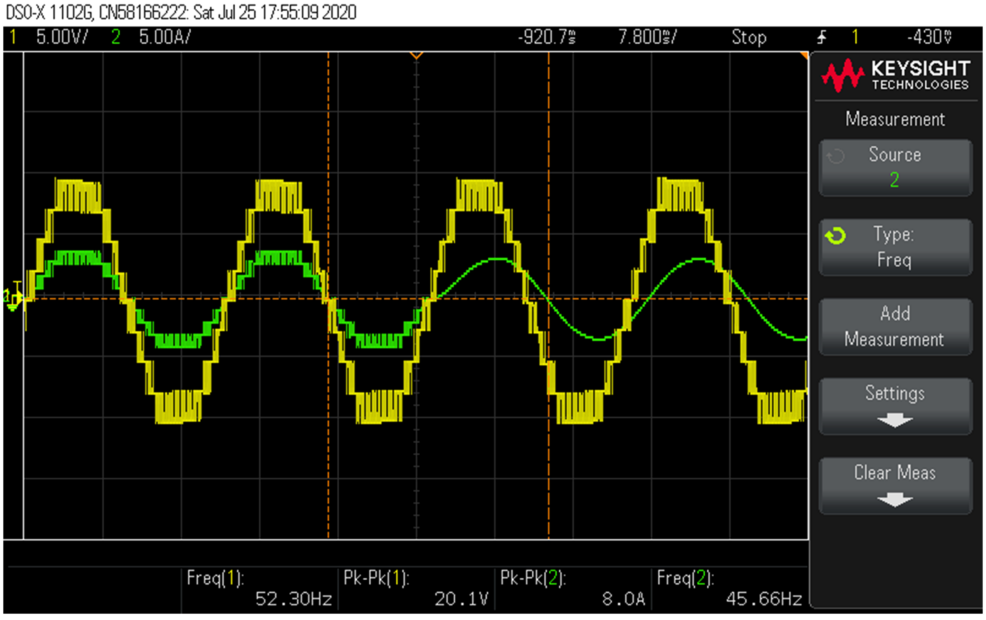


FIGURE 13 Experimental output voltage and current waveform for a load change of R = 50 Ω to R = 50 Ω L = 50 mH [Colour figure can be viewed at wileyonlinelibrary.com]

responded immediately within the cycle stepping out from staircase waveform to sinusoidal waveform, and it is visible in Figure 13.

Figure 14 shows the capacitor output voltage. It is observed that capacitor voltages C_1 and C_2 are clamped to 48.8 and 50 V sticking to the voltage balancing merit of switched-capacitor type multilevel inverter. Furthermore, the capacitor takes transient time to charge to half of the input voltage because of its internal resistance.

Figure 15 depicts voltage and current across the switch S_1 during RL load and the S_1 has to withstand a voltage stress of 102 V which is almost equal to the input voltage and it is quite evident from the waveform. The S_1 current is nearly equal to load current and negative spike is the reverse current due to inductive loading. Figure 16 depicts the voltage THD measured using the fluke power quality analyzer and the value read as 16.3% for the proposed 9L-SCMLI.

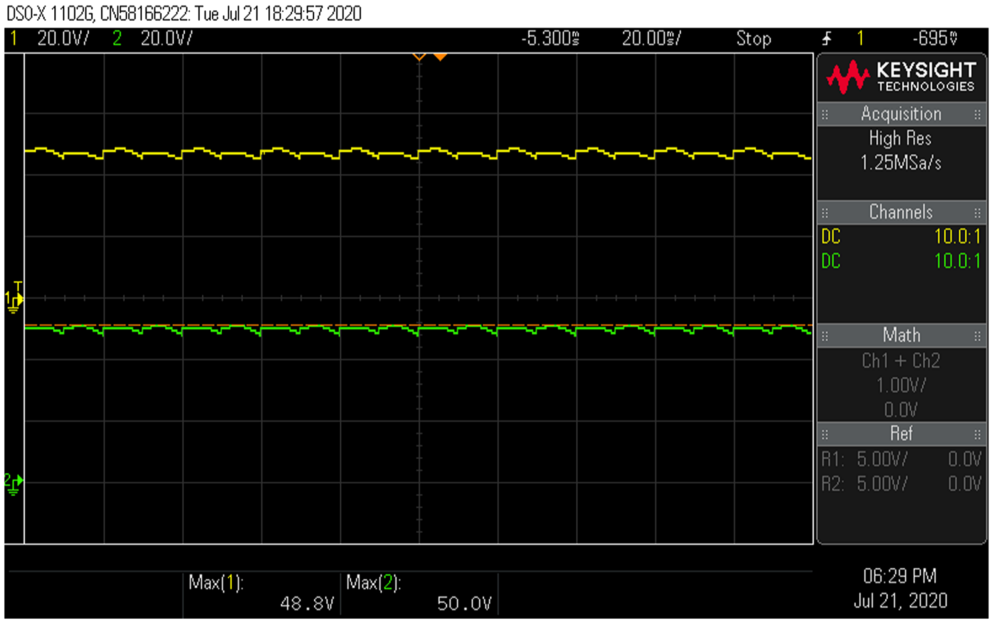


FIGURE 14 Experimental voltage waveform across the capacitors C_1 and C_2 [Colour figure can be viewed at wileyonlinelibrary.com]

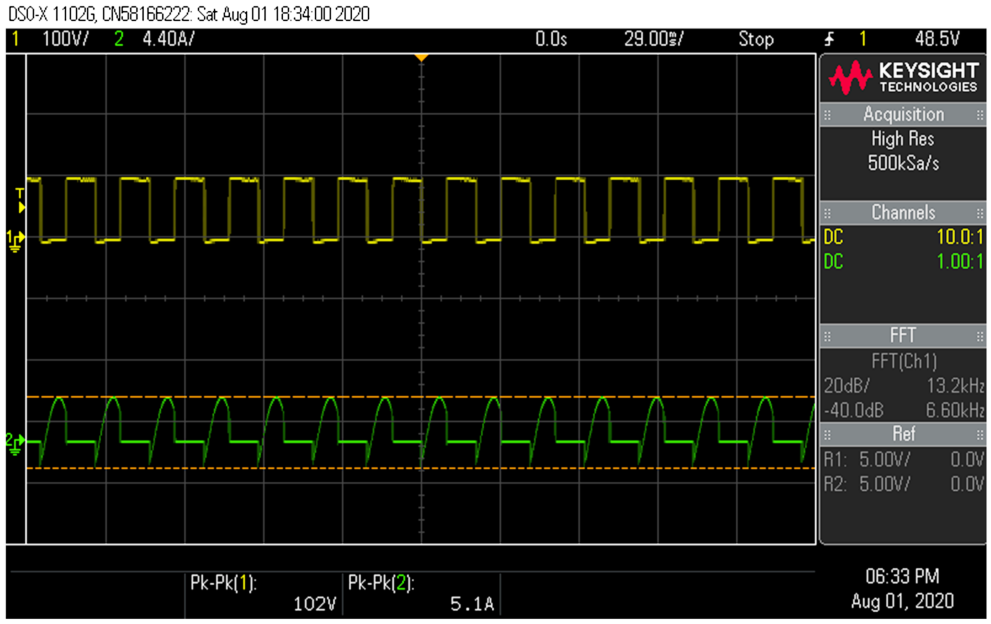


FIGURE 15 Experimental voltage and current waveform across the switch S_1 [Colour figure can be viewed at wileyonlinelibrary.com]

The on-state resistance of IGBT switches and diodes used in the experimental prototype are 14 mΩ and 3 mΩ. The peak current flowing through the switch S_1 is 2.55 A, and the blocking voltage is 102 V. On using the above data in Equations 18 and 26, the conduction loss and switching loss incurred in S_1 are estimated as 1.58 and 0.49 W, respectively.

The conduction loss, switching loss for other switches, and capacitor ripple loss for capacitors C_1 and C_2 are estimated using Equations 16–30 and plotted as graph as shown in Figure 17. From Figure 17, it is worth mentioning that the conduction loss is maximum for S_1 and S_2 because they are in conduction state for a longer period and switching loss is high for S_3 and S_4 due to frequent turn on and turn off. The efficiency of the system stood at 97.86% with a total loss of 17.65 for the 800 W 9L-SCMLI prototype.

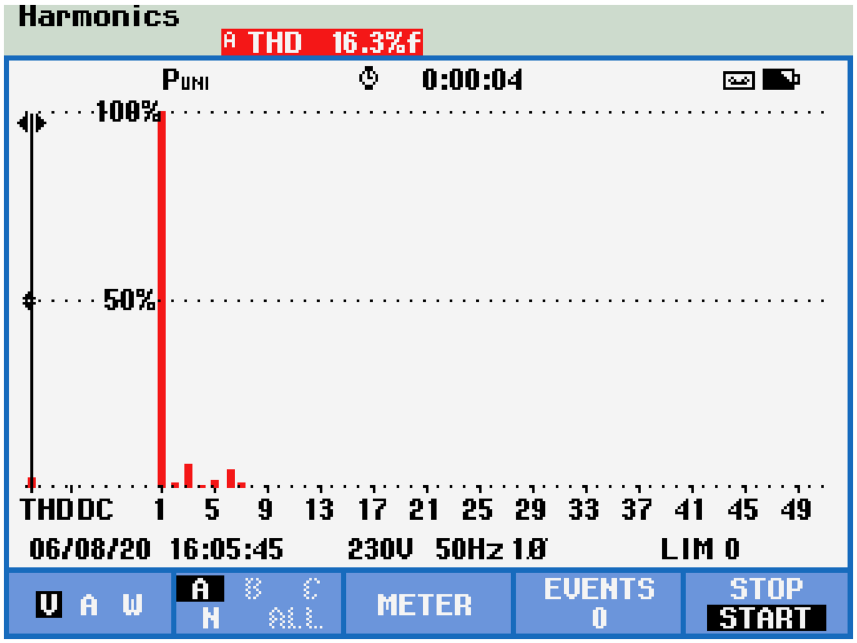


FIGURE 16 Experimental voltage THD of proposed 9L-SCMLI [Colour figure can be viewed at wileyonlinelibrary.com]

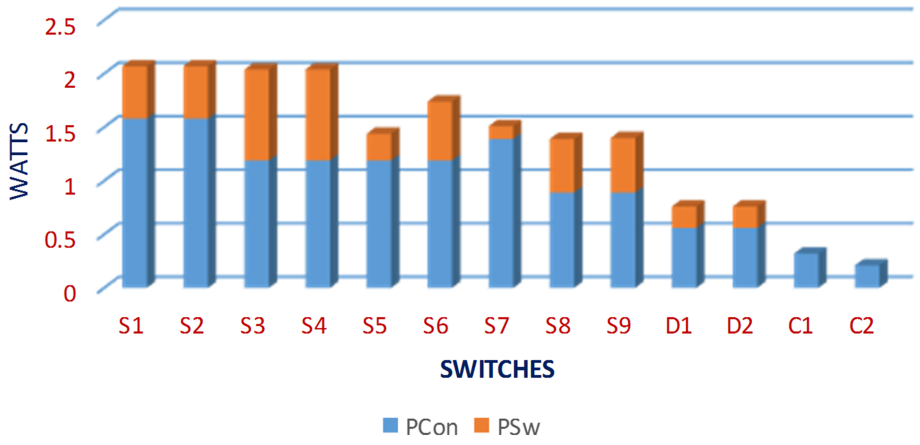


FIGURE 17 Power loss of 9L-SCMLI devices [Colour figure can be viewed at wileyonlinelibrary.com]

8 | CONCLUSION

The proposed 9L-SCMLI design has been modeled for the given specifications in MATLAB/SIMULINK software package, and several simulation trials have been made for estimating the performance analysis. From the simulation results, it has been found that the developed converter has given satisfactory multilevel voltage output with minimum harmonic distortions. This design is suitable for high voltage medium power applications. Several test runs have made with different combinations of switching sequences, and the corresponding output voltages have been captured and plotted. The proposed converter has compared with several other converters. The proposed 9L-SCMLI converter outperforms the other MLI, as discussed in the literature.

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