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# Design and development of symmetrical super-lift DC–AC converter using firefly algorithm for solar-photovoltaic applications

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**Abstract:** The super-lift technique is an exceptional contribution to DC–DC conversion technology. A replacement approach of symmetrical super-lift multilevel inverter (SLMLI) DC/AC technology is proposed with a reduced number of elements compared with the traditional multilevel inverter. In this method, the firefly algorithm conveys a leading task for the SLMLI topology for solar-photovoltaic applications. It generates low distortion output and consumes the harmonic band of the fast Fourier transform framework by the employment of the proposed algorithm. The simulation circuit for 15 levels output uses single switch super-lift inverter feed with different kinds of load (R, RL and RLE) conditions. The power quality is improved in SLMLI with minimised harmonics underneath the various modulation indices while varied from 0.1 up to 0.8. The circuit is designed in a field-programmable gate array, which includes the firefly rule to help the multilevel output, to reduce the lower order harmonics and to find the best switching angle. As a result, the minimum total harmonic distortion from the simulation and hardware circuit is achieved. Due to the absence of bulky switches, inductor and filter elements expose the effectiveness of the proposed system.

## 1 Introduction

The requirement for sustainable energy has grown up significantly over the years due to the fast depletion of fossil fuel and also the greenhouse effect. The solar cell photovoltaic (PV) module growth in India within the year 2016–2017 ranged from 2000 to 2500 MW and in the future, it would be 5000–5500 MW due to the growing demand for the energy is needed [1]. The DC-to-AC conversion techniques will be separated into two types: multilevel modulation (MLM) and pulse-width modulation (PWM). Each of these modulation schemes has a different mechanism for providing the voltage level [2]. In general, there are three sorts of traditional multilevel inverters structures such as neutral point clamped (NPC) [3], flying capacitor (FC) [4] and cascaded H bridge multilevel inverters (CHBMLIs) [5] which are notably helpful to extend the output voltage level. Over the past few years, several multilevel inverters are proposed for DC–AC conversion to solar-PV systems to achieve 15-level MLI with different load conditions [6, 7]. These conventional solar multilevel inverters (MLIs) require 28 switches and in binary, trinary mode 12 switches can be obtained, whereas as in MMC (multilevel modular conventional) method, only 7 switches are employed to achieve 15 level [8, 9]. In the cascade symmetric MLI, Odeh and co-authors [10], each module is made up of H- and half bridges, two isolated equal DC sources and a bidirectional auxiliary circuit. The reduction of the total harmonic distortion (THD) in MLIs requires resolution of complex non-linear transcendental equations with a firefly algorithm (FA) is proposed Belkacem *et al.* [11]. MLI topology has been proposed with the basic unit requires three DC voltage sources and ten switches to synthesise 15 level across the load by Siddique *et al.* [12]. The symmetrical 15-level MLI, Edwards and co-authors [13] present the DC source magnitudes are equal and the results are verified in RL load condition both simulation and hardware approaches, which vertically routines a reference waveform to achieve the desirable multilevel output waveform. The above perceptions are applicable for industrial and commercial applications such as flexible AC transmission system devices and AC drives. The disadvantages of conventional converter topology are to integrate many levels using several clamping diodes, clamping capacitors, bulky filters and DC sources and may extend the establishment zone because of the increase in-built cost of the converter and convoluted control circuits. In the symmetrical MLI technique, all the DC sources contain a unique quality that guarantees great modularity and it is the same quantity of DC voltage that is applied to the subsequent stage of the converter circuit. This multilevel inverting strategy horizontally collects levels to get the output waveform (e.g. a sine wave). The system is designed with 15-level SLMLI along with optimum control techniques like an FA rule to find the effective switching angle and THD values that compares with more than asymmetrical MLI [10, 11]. The SLMLI uses seven capacitors $C_6$, $C_7$, $C_8$, $C_9$, $C_{10}$, $C_{11}$, and $C_{12}$ which are used to split or divide the output voltage into 15 levels created by single-pole multi-through (SPMT) and double pole double through switch (2P2TS) as shown in Fig. 1. As a result, the proposed method increases the output voltage gain with modulation index (MI) limitation and reduces the voltage drop across switches ($S_1$ and $S_2$) that is comparatively beyond that of the conventional MLIs. The proposed model of the super-lift inverter is well suited for reactive power compensation and providing the desired alternating staircase output wave. The quality of end result voltage has been improved by the numerous voltages with the assistance of the least semiconductor switches. The symmetrical super-lift multilevel strategy utilises single MOSFET switch and capacitor energy banks on the grounds that solar PV source voltage might be broadened and this may create a higher incentive in output voltage by way of increasing the level.

## 2 Double-lift boost (DLB) converter

The DLB converter is modified form of the step-up boost converter. It consists of a coupled inductor, charge pump and active clamper circuits which are more complicated [12]. Here, the same method is adopted, show that the output voltage is twice greater than the input voltage source, but with the necessity of reducing module structure in the double-lift boost circuit. The input voltage source ($V_{in}$) for the converter is roughly around 42 V, when the capacitor voltage $V_{C1}$ is charged by input source ($V_{in}$), in the stable state (voltage across the capacitor) $V_{C1} = V_{input}$ and the voltage $V_1$ across the capacitor $C_2$ is


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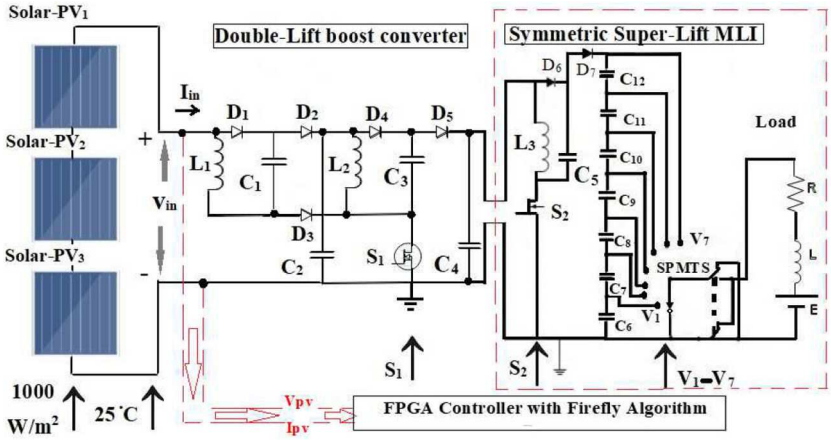



**Fig. 1** *Circuit diagram for 15-levels SLMLI*

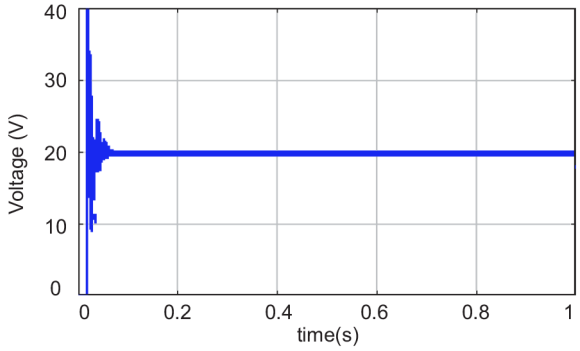



**Fig. 2** *Solar PV DC output voltage*

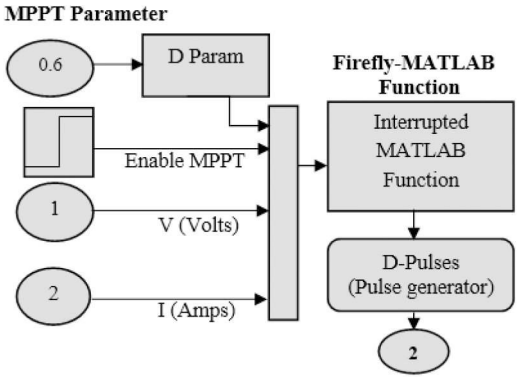



**Fig. 3** *MPPT with a firefly controller function*

$$V_1 = \frac{2-k}{1-k} V_{\text{in}} \tag{1}$$

The number of node voltages is from $V_7$ up to $V_1$. The purpose of the capacitor voltage ($E_{\text{m}}$) for each capacitor is to function as a capacitor energy bank

$$E_{\text{m}} = \frac{V_{\text{dc}}}{N-1} \tag{2}$$

where $N$ denotes the number of levels. The capacitor band switch or single pole multi-through switch (SPMTS) turn on positive charging output terminal voltage from $V_7$, $V_6$, $V_5$, $V_4$, $V_3$, $V_2$, $V_1$, $V_0$ and negative discharging output terminal voltage turn off are $-V_1$, $-V_2$, $-V_3$, $-V_4$, $-V_5$, $-V_6$, and $-V_7$, respectively, in SLMLI. It has been furthermore analysed and developed by using MATLAB/Simulink software. The hardware implementation of FPGA is better power quality improvement with FA support of finding the best THD and switching angle values. The prototype model suits reactive compensation and the present inverter circuit minimises electromagnetic interference problem with the help of the main capacitor bank ($C_6$–$C_{12}$), and it is used in medium and low power applications, particularly in renewable power electronics utility.

The capacitor voltage $V_{C3}$ is charged by $V_1$. When current passing through inductor $L_2$ with increased voltage $V_1$, switch ($S_1$) is in ON mode ($KT$). When it decreases with the voltage level – ($V_{\text{out}}$–$2V_{\text{input}}$), during the switch $(1-k)T$ off period, the ripple of the inductor current ($iL_2$) is

$$\Delta iL_2 = \frac{V_1}{L_2} KT + \frac{V_0 - 2V_1}{L_2} I_{L1}(1-K)T, \tag{3}$$

$$V_0 = \frac{2-k}{1-k} = \left(\frac{2-k}{1-k}\right)^2 V_{\text{in}}, \tag{4}$$

where $K$ is the duty cycle and the voltage transfer gain

$$G = \frac{V_0}{V_{\text{in}}} = \left(\frac{2-k}{1-k}\right)^2 \tag{5}$$

The variant ratio of current $iL_1$ through inductor $L_1$ is

$$\xi_1 = \frac{\Delta iL_{1/2}}{iL_1} = \frac{K(2-K)TV_{\text{in}}}{2L_1 I_0} = \frac{K(1-K)^2}{2(2-K)^3} = \frac{R}{fL_1}. \tag{6}$$

The variant ratio of current $iL_2$ through inductor $L_2$ is

$$\xi_1 = \frac{\Delta iL_{1/2}}{iL_1} = \frac{K(1-K)TV_1}{2L_2 I_{\text{in}}} = \frac{KTV_0(1-K)^2}{2(2-K)^3 L_2 I_0} = \frac{K(1-K)^2 R}{2(2-K)fL_2}. \tag{7}$$

Therefore, the variant ratio of output voltage $V_0$ is

$$\varepsilon = \frac{\Delta V_{0/2}}{V_0} = \frac{k}{2Rfc_4} \tag{8}$$

The maximum induced voltage and currents from MPP passing through the next stage of converters are provided. The performance of the DLB converter yields the output voltages of ($V_{\text{out}}$) 60 V which were developed by two important parameters, namely inductors ($L_1$, $L_2$) and capacitors ($C_1$, $C_2$ and $C_3$).

## 3 PV source and modulation scheme

The input sources from solar PV are connected with the double-lift boosted DC–DC converter, which works and lifts up a voltage which is encouraged into the super lift MLI. The simulation method of solar-PV array modules is used in sun power SPR 305-WHT and the number of cells per module using 96 cells. The solar cell module two connections are followed by the combination of series and parallel connected modules. The solar PV array module


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**Table 1** Comparison of 15-level traditional MLI with symmetrical SLMLI

| MLI | Total number of stages | Total number of main diodes | Total number of switches | Total number of clamping diodes | Total number of DC bus capacitor | Total number of balancing capacitors |
|---|---|---|---|---|---|---|
| NPC | 7/15 level | 6/28 | 6/28 | 10/182 | 0/14 | 6/0 |
| FC | | 0/28 | 6/28 | 6/0 | 5/14 | 6/91 |
| CHB | | 0/12 | 12/28 | 12/0 | 3/7 | 0/0 |
| proposed SLMLI | | 2/2 | >1/1 | >2/2 | >3/14 | >1/1 |

is designed as Solar-$PV_1$, Solar-$PV_2$, and Solar-$PV_3$ made by supply (14 V*3) 42 V and 4.05 A. Here, the terminal voltage is equal to the constant MPP. The solar PV output voltage is shown in Fig. 2. The above three PV modules are adjusted to fit the characteristics measured standard test condition with irradiation key parameters like 1000 W/$m^2$, temperature 25°C, and nominal operating cell temperature 45°C. The parameter for open-circuit voltage is (21.4 V*3) 64.2 V and short-circuits current is 5.96 A.

Record-low temperature: −10°C.
Temperature coefficient of ($V_{OC}$): −(0.30)%/°C.
Module open-circuit voltage ($V_{OC}$): 20 V.
Inverter maximum input voltage: 60 V.

The STC temperature is 25°C. This temperature needs to be deducted from the array location's record-low temperature of −10° as follows:

25 − (−10) = 35° difference.

Multiply the 35° difference by the temperature coefficient of $V_{OC}$, then multiply by the module's $V_{OC}$

35 × 0.0030 = 0.105.
0.105 × 20 V = 2.1 V.

The number of PV modules will be increased due to record-low temperatures. After adding the increase in voltage to single PV module $V_{OC}$, then divide the inverter maximum input voltage by module $V_{oc}$. This will give the maximum number of modules that can be wired in a series string per that inverter and specific location.

2.1 V + 20 V = 22.1 $V_{Max}$

60 V/22.1 = 2.71 (round down to a whole number) the maximum number of modules in this series string is 2.71. A series string of three could potentially produce >60 V during record-low temperatures. (As per our paper presents in three solar PV string modules, as shown in Fig. 1) The quantity of modules wired in series multiplied by the $V_{max}$ equals maximum system voltage 3×22.1 = 66.3 V maximum system input voltage.

The perturb and observe rule is supported to create the duty cycle of both the converter and also the SSLMLI. The aim of the MPP rule is to incorporate a variety of upper, lower limit (*D*-max) values and incremental, step-by-step values (Delta-*D*) which helps to find the most effective optimum converter duty cycle (*D*).

### *3.1 MPPT parameter*

The pulse generator using firefly Matlab functions is fed into both DLB converter and SLMLI switches in Fig. 3. The FA program has performed varying the MI across the MLI switches, herewith producing appropriate SLMLI output and THD values.

## 4 Symmetrical SLMLI

An approach has been created with SLMLI, which constructed from a modified voltage-lift Luo (DC/DC) converter [13]. The input sources from solar PV are fed with double-lift boost DC–DC converter, which is operated maximise DC voltage fed into an SLMLI. The multilevel electrical converter based on DC sources leads in two cases:

(i) Symmetrical type MLI.
(ii) Asymmetric type MLI.

The asymmetric MLI has been investigated a maximum number of levels obtained with a high number of switches and gate driver circuits for generating all levels [14]. Here, symmetric MLI minimum number of levels is applied to achieve maximum output voltage. The solar PV system is used three number of (Solar-PV1 up to Solar-PV3) modules. The symmetrical SLMLI consists of single MOSFET switch S2, and main capacitors $C_6$–$C_{12}$ combined with SPMT switch (SPMTS). As the most important part of SLMLI, the number of required switches against the required voltage level is an extremely important element within the design. In this regard, the SLMLI produces a large number of multilevel outputs is increased by using multiple capacitors without increasing the number of bridges or power circuit topology. The advantage of this proposed topology is that it's less apparatus and reduced voltage stress across the main capacitor bank.

### *4.1 Modified SLMLI design*

This module basically consists of only one MOSFET switch, two freewheeling diodes and seven parallel main switching capacitors to generate 15-level output (+ 7 V, 0 and − 7 V), ( +6 V, 0 and −6 V), ( +5 V, 0 and −5 V), ( +4 V, 0 and −4 V), ( + 3 V, 0 and −3 V), ( +2 V 0 and −2 V), ( +1 V, 0 and −1 V), whereas traditional MLIs NPC, FC and CHB require 28 switches to generate the 15 level output shown in Table 1. A number of levels used for increasing multiple capacitors to achieve maximum output voltage to attain less THD. A number of the capacitor devices are connected in series so that the voltage stress across the devices could be reduced. With this, connection formulated symmetrical multilevel (DC–AC) inverter number of levels has been increased as mentioned below, where *C* indicates the number of capacitors adding with the single switch used in the proposed SLMLI suitable and particularly for solar PV renewable energy application

$$N \text{ level} = 2C + 1.$$

Proposed circuit

$$N \text{ level} = 2(7) + 1 \text{ switch} = 15 \text{ levels} \quad (9)$$

$$2(3 \text{ capacitor}) + 1S = 7 \text{ level} \quad (10)$$

$$2(10 \text{ capacitor}) + 1S = 21 \text{ level} \quad (11)$$

$$2(12 \text{ capacitor}) + 1S = 25 \text{ level} \quad (12)$$

$$2(17 \text{ capacitor}) + 1S = 35 \text{ level} \quad (13)$$

$$(13)2(22 \text{ capacitor}) + 1S = 45 \text{ level} \quad (14)$$

Here, 15-level SLMLI can be applied. When the main switch S2 is on, the inductor ($L_3$), and capacitor ($C_5$) are charged by the source voltage (VDC input) during switch-on period *kT*. The end result voltage $V_{out}$ is highly raised from the source voltage because of inductor $L_3$ and capacitor $C_5$, when the main switch during off


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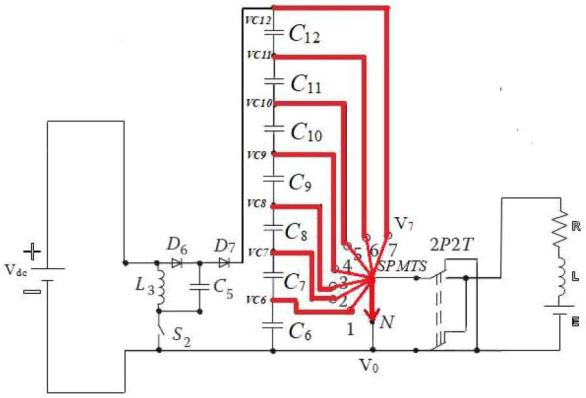



**Fig. 4** *ON-state SLMLI*

**Table 2** Deviation report of PV module with/without MPPT

| Description | Without MPPT using SLMLI | With MPPT using SLMLI |
|---|---|---|
| maximum power ($P_{max}$) | 69–70 W | 75 W |
| voltage at $P_{max}$ ($V_{mp}$) | 20 V | 21.1 V |
| current at $P_{max}$ ($I_{mp}$) | 4.25 A | 4.96 A |
| open-circuit voltage ($V_{oc}$) | 21.5 V | 22.1 V |
| short-circuit current ($I_{sc}$) | 4.51 A | 5.96 A |

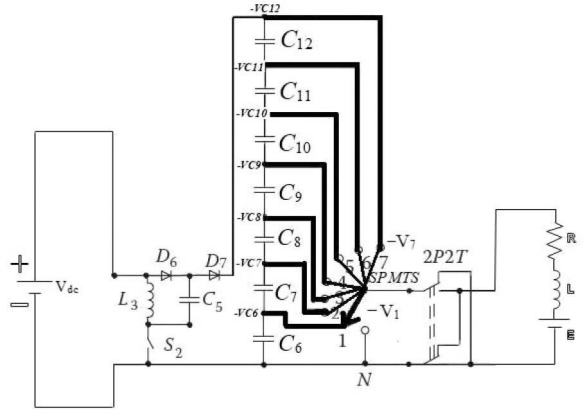



**Fig. 5** *OFF-state SLMLI*

period $(1-k)T$ decreases voltage level $-(V_{out}-2V_{input})$. This symmetric MLI operates in SPMTS with different load conditions. The number of voltage increases when the harmonic content of the voltage is decreased. Therefore ripple current of the inductor $iL$ equation can be given as

$$\Delta iL_1 = \left(\frac{V_{in}}{L}\right)KT = \left[\frac{V_0 - 2V_{in}}{L}\right]KT \tag{15}$$

## 5 SLMLI modes of operation

### 5.1 ON-state MLI

The output voltage switch position ($V_7$) is in charging mode, when it is at the node in between $D_7$ (diode) and $C_{12}$ (capacitor), there will be a potential voltage across the capacitor $V_{c12}$ which is named as $V_7 = +1/7V_{dc}$ under the condition, 2P2T switch is closed as shown in Fig. 4. It is taken as the exact charging output voltage for the positive half cycle of the load. The same process should be followed:

- $V_6 = +1/6V_{dc}$, when it is at the node in between the capacitors $C_{12}$ and $C_{11}$, there will be a potential voltage across the capacitor $V_{c11}$.

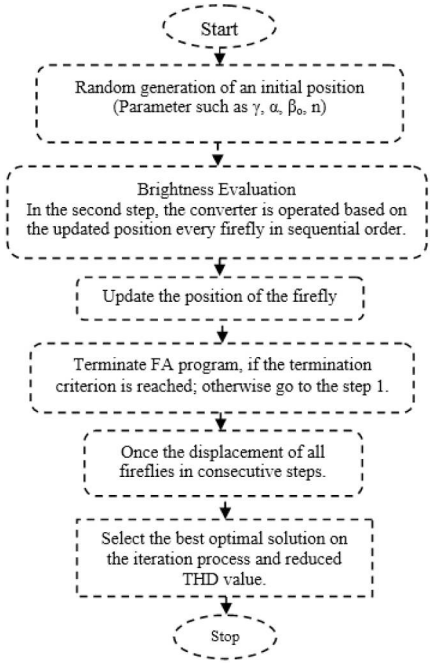



**Fig. 6** *Procedure of FA applies to minimal THD reduction*

- $V_5 = +1/5V_{dc}$, when it is at the node in between the capacitors $C_{11}$ and $C_{10}$, there will be a potential voltage across the capacitor $V_{c10}$.
- $V_4 = +1/4V_{dc}$, when it is at the node in between the capacitors $C_{10}$ and $C_9$, there will be a potential voltage across the capacitor $V_{c9}$.
- $V_3 = +1/3V_{dc}$, when it is at the node in between the capacitors $C_9$ and $C_8$, there will be a potential voltage across the capacitor $V_{c8}$.
- $V_2 = +1/2V_{dc}$, when it is at the node in between the capacitors $C_8$ and $C_7$, there will be a potential voltage across the capacitor $V_{c7}$.
- $V_1 = +1/1V_{dc}$, when it is at the node in between the capacitors $C_7$ and $C_6$, there will be a potential voltage across the capacitor $V_{c6}$ and finally, the SPMTS is at a point $V_0$.

$V_0 = 0$ (neutral) when it is at the node in between $C_6$ and $V_0$, there will be a potential voltage across the output that will be followed through a 2P2TS that will be passing to the next state of the load. The symmetric SLMLI switching methods are shown in Table 2.

### 5.2 OFF-state MLI

The output voltage switching position $(-V_1)$ is in discharging mode, when it is at the node in between $N$(neutral) and $C_6$, there will be potential drop across the capacitor $V_{c6}$, which is named as $-V_1 = -1/V_{dc}$ and under the condition, 2P2T switch is closed as shown in Fig. 5. It is taken as the exact discharging output voltage for the negative half cycle of the load. The same process should be followed:

- $-V_2 = -1/2V_{dc}$, when it is at the node in between the capacitors $C_6$–$C_7$, there will be a potential drop across the capacitor $(-V_{c7})$.
- $-V_3 = -1/3V_{dc}$, when it is at the node in between the capacitors $C_7$–$C_8$, there will be a potential drop across the capacitor $(-V_{c8})$.
- $-V_4 = -1/4V_{dc}$, when it is at the node in between the capacitors $C_8$–$C_9$, there will be a potential drop across the capacitor $(-V_{c9})$.
- $-V_5 = -1/5V_{dc}$, when it is at the node in between the capacitors $C_9$–$C_{10}$, there will be a potential drop across the capacitor $(-V_{c10})$.


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**Table 3** Inverter switching method of 15-level SLMLI

| S. no | Main capacitor bank SPML<br>Output voltage switch point (SPMTS) | Modes of operation<br>ON | Switch ON state | Main capacitor bank single-pole multi-terminal output voltage switch<br>Point (SPMTS) | Modes of operation<br>OFF | Switch OFF state |
|---|---|---|---|---|---|---|
| 1. | $V_7$ | I | $+1/7V_{dc}$ | $-V_7$ | XV | $-1/7V_{dc}$ |
| 2. | $V_6$ | II | $+1/6V_{dc}$ | $-V_6$ | XIV | $-1/6V_{dc}$ |
| 3. | $V_5$ | III | $+1/5V_{dc}$ | $-V_5$ | XIII | $-1/5V_{dc}$ |
| 4. | $V_4$ | IV | $+1/4V_{dc}$ | $-V_4$ | XII | $-1/4V_{dc}$ |
| 5. | $V_3$ | V | $+1/3V_{dc}$ | $-V_3$ | XI | $-1/3V_{dc}$ |
| 6. | $V_2$ | VI | $+1/2V_{dc}$ | $-V_2$ | X | $-1/2V_{dc}$ |
| 7. | $V_1$ | VII | $+1/1V_{dc}$ | $-V_1$ | IX | $-1/1V_{dc}$ |
| 8. | $V_0$ | VIII | 0 | $-V_0$ | VIII | 0 |

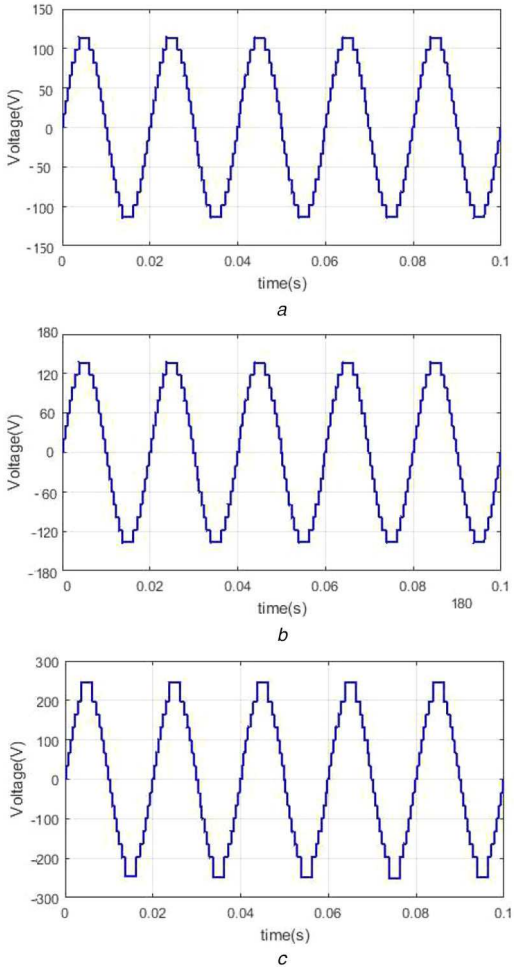



**Fig. 7** *Output voltage waveform of*
***(a)*** R load, ***(b)*** RL load, ***(c)*** RLE load

- $-V_6 = -1/6V_{dc}$, when it is at the node in between the capacitors $C_{10}$–$C_{11}$, there will be a potential drop across the capacitor ($-V_{c11}$) and finally, the SPMTS is at a point ($-V_7$).
- $-V_7 = -1/7V_{dc}$, when it is at the node in between the capacitors $C_{11}$–$C_{12}$, there will be a potential drop across the capacitor ($-V_{c12}$). It will be followed 2P2T switch and passing through to the next state of the load.

## 6 Implementation of FA

The interpreted MATLAB function of the firefly algorithmic program developed by Xian she yang in 2007–2008, which was made on flashing patterns and behaviour of firefly. It is basic to attract mating partners to seek out the best solution among the

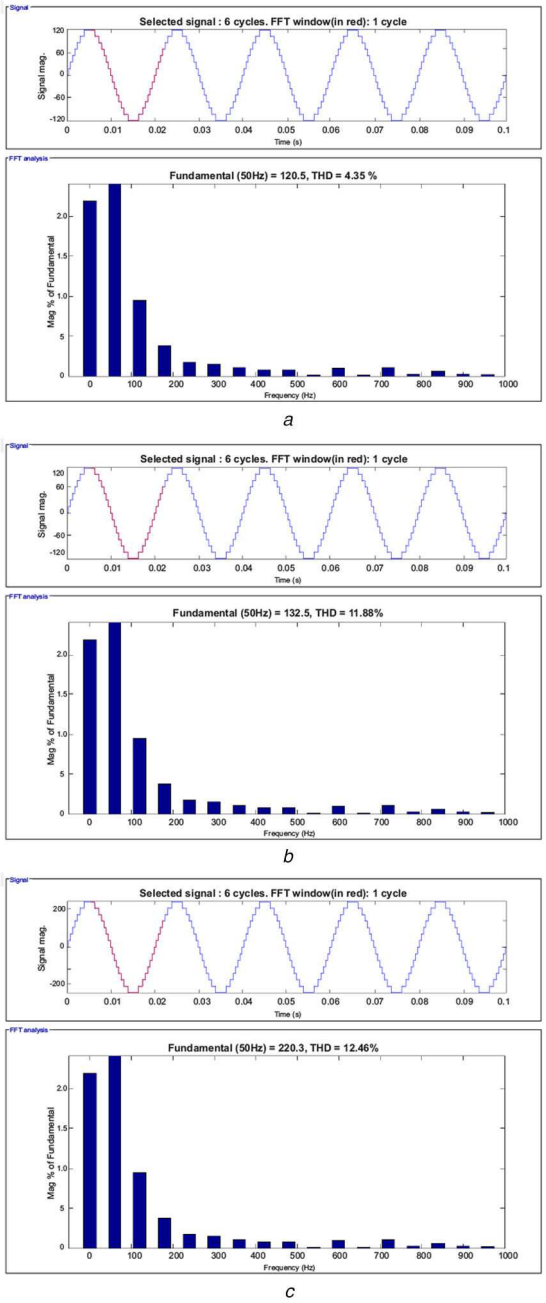



**Fig. 8** *THD analysis of*
***(a)*** R load, ***(b)*** RL load, ***(c)*** RLE load

population and generate pulses of both double boost converter and SSLMLI. The firefly rule can deal with non-linear and multimodal


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**Table 4** Implementation parameters of FA

| Description | Value |
|---|---|
| maximum generation ($\gamma$) | 10 |
| population ($p$) | 20 |
| alpha ($\alpha$) | 1 |
| attractiveness ($\beta_0$) | 50 |
| number of fireflies ($n$) | 100 |

**Table 5** THD analysis of R, RL and RLE

| Modulation index | Optimisation tuning | THD, % | | | Optimum switching angle with MI | (Load) THD% |
|---|---|---|---|---|---|---|
| | | RLE | RL | R | | |
| 0.8 | FA | 29.46 | 21.88 | 19.35 | $\alpha_1 = 18.95$, $\alpha_2 = 21.50$, | R load |
| 0.7 | | 12.46 | 12.74 | 13.92 | $\alpha_3 = 33.91$ (MI = 0.45) | 9.35% |
| 0.6 | | 14.39 | 14.65 | 11.81 | $\alpha_1 = 16.05$, $\alpha_2 = 19.21$, | RL load |
| 0.5 | | 15.79 | 16.22 | 17.76 | $\alpha_3 = 31.54$ (MI = 0.27) | 11.88% |
| 0.4 | | 16.00 | 15.50 | 9.35 | | |
| 0.3 | | 17.19 | 13.80 | 15.90 | $\alpha_1 = 5.37$, $\alpha_2 = 19.21$, | RLE load |
| 0.2 | | 19.21 | 11.88 | 16.01 | $\alpha_3 = 43.54$ (MI = 0.72) | 12.46% |
| 0.1 | | 21.99 | 18.16 | 18.15 | | |

**Table 6** Simulation parameter of symmetric type of super-lift MLI

| S. no | Parameter Name | Range |
|---|---|---|
| 1. | open-circuit voltage ($V_{OC}$) | 64.2 V |
| 2. | short-circuit current ($I_{SC}$) | 5.96 A |
| 3. | inductor | 540 mH |
| 4. | capacitor (DC–DC) | 850 μF |
| 5. | capacitor bank (DC–AC) | 2600 μF |
| 6. | R load | 30 Ω |
| 7. | RL load | 30 Ω, 40 mH |
| 8. | RLE load | 30 Ω, 40 mH, 220 V |

optimisation issues. It does not use the velocity function and there are no issues as those associated with GA and PSO.

*Step 1: Initialisation:* In the initial process, the PV current and voltage are initialised the algorithm parameters such as $\beta_0$, $n$, $\alpha$, $\gamma$, (population size) $N$ and the termination criterion. Here, the firefly initial position is assumed to be a switching angle of the multilevel converter. In addition, the brightness of every firefly is taken as generated solar (PV) power $P_{pv}$ 14 V, corresponding to the position of this firefly. The fireflies are two fundamental functions, such as generate bioluminescence flashes to draw in matting partners and to draw in potential prey. The initialise objective function is

$$I(r) = \left(\frac{I_s}{r^2}\right) \tag{16}$$

where $I_r$ is the intensity of the source, $r$ is the observers distance from the source.

*Step 2: Brightness evaluation:* In this second step, the multilevel converter is operated based on the updated position of each and every firefly in sequential order. For each switching angle, the corresponding PV output power, $P_{pv}$ is taken as the brightness or light intensity of the respective firefly. This step is repeated for the position of all fireflies in the population. Now determine the light intensity of each of the fireflies to find out the brightness of every firefly.

$$I = I_0 e^{\gamma r^2} \tag{17}$$

If we have a tendency to take absorption coefficient $\gamma$ into account. The light intensity $I$ varies with the square of the distance $r$.

*Step 3: Update the position of fireflies and termination:* The firefly with better brightness remains in its position and the remaining other fireflies update their position. Terminate the program if the termination criterion is reached. Otherwise, attend step one. The optimisation firefly algorithm rule is terminated once the dislocation of all fireflies in consecutive steps attained a predefined set reduce value. Once the program is terminated, the initialise firefly population by considering the subsequent equation

$$x_{t+1} = x_t + \beta_0 e^{-\gamma r^2} + \alpha\varepsilon \tag{18}$$

where the second term is because of the attraction and the third term is randomisation with being the randomisation parameters. Calculate the attractiveness of firefly is

$$\beta = \beta_0 e^{-\gamma r^2} \tag{19}$$

Movement of few brighter fireflies towards brighter one, the movement of firefly $I$ is attract to a different additional attractive (brighter) firefly. $J$ is the determine by

$$x_t = x_t + \beta_0 e^{-\gamma r i,j}(xj - xi) + \alpha\varepsilon \tag{20}$$

Finally, update the light-weight intensives of fireflies and rank the fireflies. Once ranking of the fireflies, find the current optimum solution shown in Fig. 6. In Table 3, the firefly implementation values of MATLAB/Simulink platform have been given below.

## 7 Simulation result and discussion

The paper deals with the 15-level symmetrical form of SLMLI assist FA program by using Matlab/Simulink code. The code will realise the optimum MI solution that depends on the switching angle of SLMLI. The individual input supply (PV) is directly connected to a double boost converter and it's a series-connected into MLI. This SLMLI simulation is performed with an output frequency of 50 Hz and a switch frequency of 5000 Hz. Their


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**Table 7** Performance analysis optimum success rate of FA, GA and PSO

| Algorithms/functions | Number of Particles | Time taken | GA, % | PSO, % | FA, % |
|---|---|---|---|---|---|
| Michalewicz ($d = 16$) [15] | 50 | 2 | 95 | 98 | 99 |
| Rosenbrock ($d = 16$) [16] | 50 | 6 | 90 | 98 | 99 |
| Dejong ($d = 256$) [17] | 50 | 7 | 100 | 100 | 100 |
| Schwefel ($d = 128$) [11] | 50 | 4 | 95 | 97 | 100 |
| Ackley ($d = 128$) [18] | 50 | 4 | 90 | 92 | 100 |
| Rastrigin [19] | 50 | 2 | 77 | 90 | 100 |
| Easom [20] | 50 | 4 | 92 | 90 | 100 |
| Griewang [21] | 50 | 1 | 90 | 92 | 100 |
| Shubert ($d = 18$) [22] | 50 | 2 | 89 | 92 | 100 |
| Yang ($d = 16$) [23] | 50 | 2 | 83 | 90 | 100 |
| proposed (SSLMLI) | 100 | 2 | 86 | 95 | 99 |

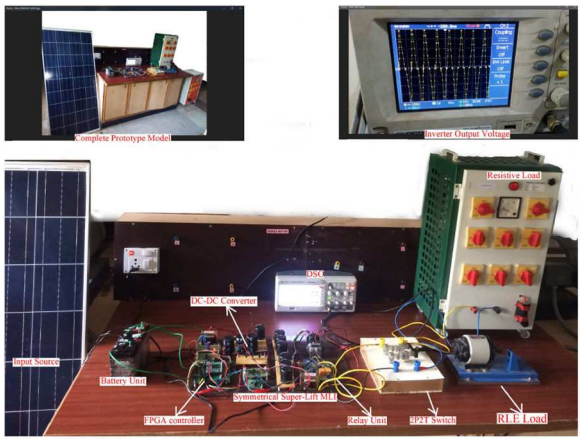
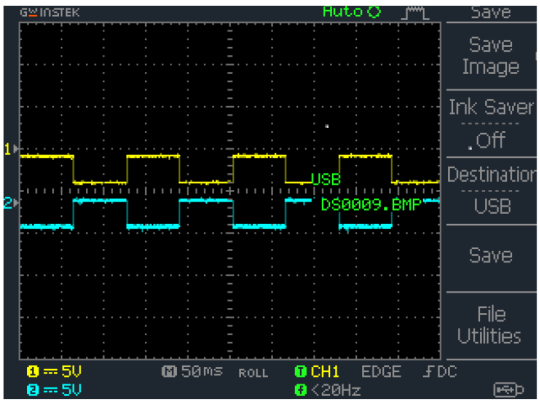
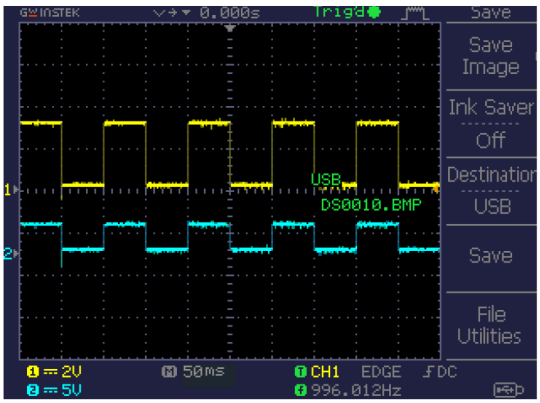



**Fig. 9** *Proposed FPGA Xilinx-3 AN Kit assist symmetrical SLMLI photography view*




*a*




*b*

**Fig. 10** *Relay unit pulses- positive half cycle and negative half cycle*
***(a)*** Relay unit pulses positive half cycle 1, ***(b)*** Relay unit negative half cycle 2

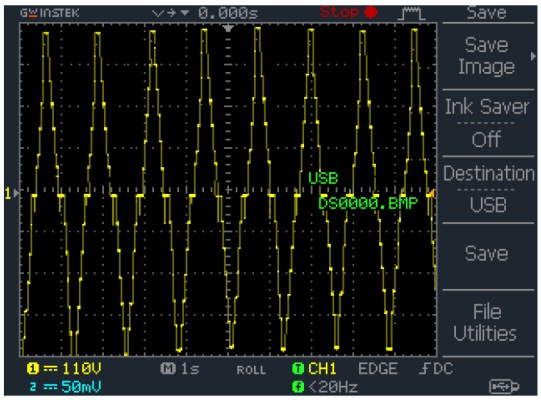



**Fig. 11** *Prototype multilevel output of symmetrical super-lift inverter*

corresponding SLMLI electrical converter output voltage R, RL and RLE are shown in Figs. 7*a–c*. The THD level obtained here is 9.35% R load in Fig. 8*a*, 11.88% RL load in Fig. 8*b* and 12.46% of the RLE load in Fig. 8*c*.

The simulation parameters of SLMLI are shown in Table 4. The FA is a much higher attainment level economically to find the best switching angle related to different load versus THD level presented in Table 5. The ranges of MI vary from 0.1 up to 0.8 for corresponding switching angles are evaluated with the firefly formula presented (Section 6). The speed of convergence of the firefly program for obtaining THD gives a very high performance within the chance of finding the global optimising solution associated with both GA and PSO, as discussed [24–26]. The FA used to reduce THD; however, there is an increase in potential level, which is compared with earlier results of metaheuristic non-linear and discrete optimisation algorithms were approached and verified [16, 17]. In our proposed work, the MPPT using symmetrical SLMLI is associated with firefly implementation as compared with the existing methodology. The parameters are shown in firefly algorithm (FA) maximum generation 10, population 20 and number of fireflies 100; it was quite updated the light intensives of ranking the firefly and the optimum solution is found with minimum time of interval (Tables 6–7).

In the earlier firefly approach of the symmetrical 15-level inverter has a low THD level, which significantly decreases 22–16% [11]. In our proposed symmetric 15-level MLI with reduced THD level around minimum level 4.35% (R load), 11.88% (RL load) and 12.46% (RLE load) has been presented. The main drawback of non-linear loads is the generation of harmonic current in addition to the original AC current. In the non-linear load, the distortion level increases in RL and RLE load conditions is due to the change of impedance value across the load. The improvement of reactive power (VAR) variation in the RL and RLE load by eliminating the negative sequence discharging current in the MLI with the help of the DC-link capacitor unit in order to keep the stable system.

## 8 Hardware result and discussion


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The SLMLI is used to test FA rule tuned with FPGA control signal access to operate the RLE motor load condition shown in Fig. 9.

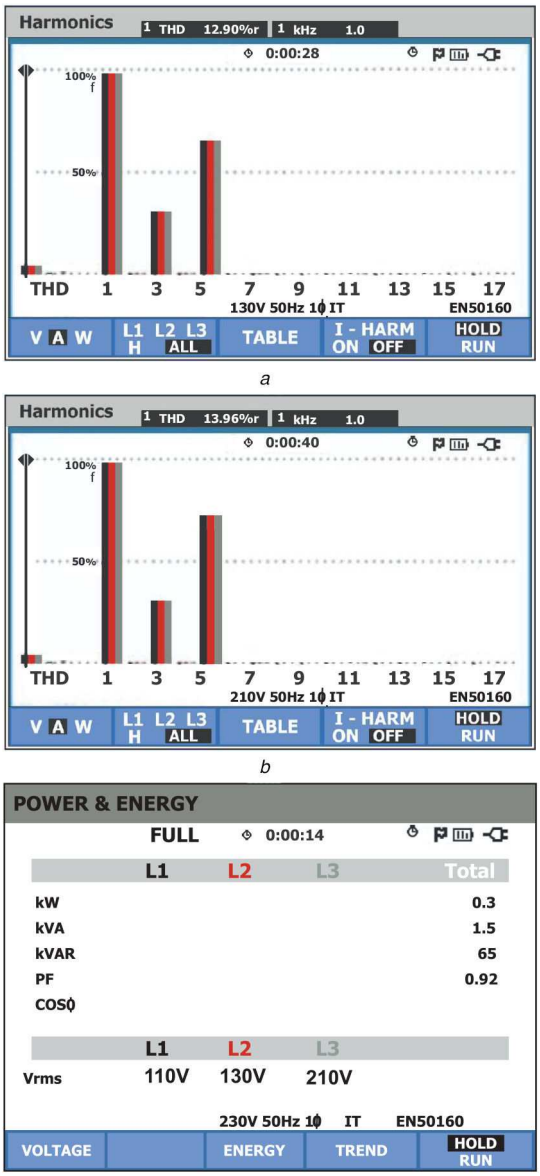



**Fig. 12** *THD spectrum of experimental output voltage*

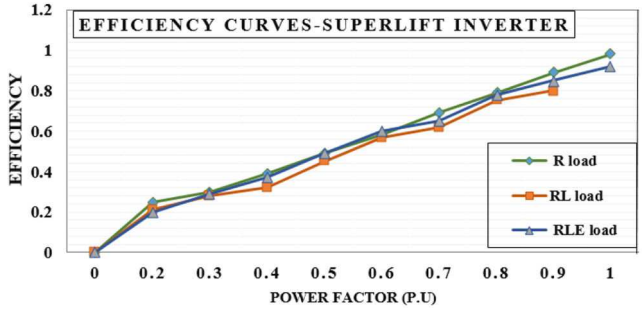



**Fig. 13** *Efficiency versus power factor curves*

The maximum power point (MPP) voltage given by PV cell ranges is based on the atmospheric situations. The ideal voltage levels are not received while the MI movements are under a critical limit. In case there are 15-level symmetric MLIs, the critical value of the MI is 0.8. When the MI moves above that value, the switches turn into the lower voltage; therefore, symmetrical SLMLIs are turned off. The values of MI are calculated from the below:

$$\mathrm{MI} = \left(\frac{V_{\mathrm{ref}}}{V_{\mathrm{carrier}}}\right) \tag{21}$$

The PV parameter is chosen as an open-circuit voltage of 48 V and a short circuit current of 3.5 A. The prototype is verified under working day time. The MPP ranges are based on the irradiance and temperature variations. In general, the DC–DC converter consists of one MOSFET switch (S1) operating frequency range at 1 kHz and the proposed multilevel inverter uses only a single MOSFET switch (S2) where pulses form FPGA board clock frequency up to 50 MHz. The Xilinx Spartan 3AN kit is verified VHDL program assists with FA. The voltage across the switching diodes of both DLB converter and SLMLI is 0.7 V. This prototype model of SLMLI is turning on MOSFET-IRFP460 through the voltage in series and along with main capacitor bank (1000 µF) or SLMLI capacitor bank $C_6$–$C_{12}$. The first half cycle positive sequence is made up of electronic relay (KEMET-EE2 series) 2P2T switch unit. The relay unit pulses are functioning at 50 ms and the operating frequency from 20 to 996 Hz as shown in Figs. 10*a* and *b* and the same process are to be continued from the main capacitors ($C_6$–$C_{12}$) during the negative phase sequence; they are discharged by the 2P2T relay unit switch. This type of electronic relay uses multiple contacts suitable for electronic switching systems and low magnetic interference benefits. These relay units have the maximum capacity of 60 W, 2 A. The RLE load across the SLMLI output voltage as shown in Fig. 11. The results of the staircase output voltage are obtained as 210 V for RLE motor load condition, 130 V for RL load and 110 V for R load, with the support of FA. The reactive power will be enhanced from 50 to 65 VAR in different types of operational load conditions. It gives a minimum THD value of 13.96, 12.90 and 5.96% in the bandwidth of spectrum varying from 1 to 5 kHz as shown in Fig. 12 and Table 8. The reactive power is to support the electrical system, when the renewable PV system is integrated with the off-grid, capacitive, resistive, and inductive load. The proposed SLMLI efficiency curves (R, RL, and RLE load) are shown in Fig. 13. However, the THD level is increased in RL, RLE load due to the absence of filter components.

The blocking voltage across each semiconductor device must be minimised with the main capacitor bank. It helps to generate reactive power to meet the demand of the inductive loads. This will keep that reactive power from having to flow all the way from the utility to the loads (RL, RLE).The optimum switching angle is produced from the firefly program to assist the load voltage with minimised THD, at the same time much development of power factor improvement. The voltage lifting technique DC/DC is successfully employed in a super-lift multilevel converter [26–28]. Where the conversion is generally focused arithmetic (or) geometric progression in power series, the aim of this function is multiple repeating parts. To validate this proposed model, the 15-level case reduces devices that have been developed and it minimise switching stress with low distortion output. Therefore, the symmetrical SLMLI stage grows up to 21, 25, 35 and 45 level series, the output voltage furthermore varies to reduce THD using medium and low power applications.

**Table 8** Comparison between experimental and simulated THD results

| S. no | R load (THD %) | $V_{\mathrm{rms}}$, V | RL load (THD %) | $V_{\mathrm{rms}}$, V | RLE load (THD %) | $V_{\mathrm{rms}}$, V |
|---|---|---|---|---|---|---|
| 1. | Simulation output voltage with different load condition | | | | | |
| | 4.35 | 120 | 11.88 | 132 | 12.46 | 220 |
| 2. | Hardware output voltage with different load condition | | | | | |
| | 5.96 | 110 | 12.90 | 130 | 13.96 | 210 |


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## 9 Conclusion

In this paper, a 15-level symmetrical form of super-lift MLI has been applied with FA and FPGA strategy equipment, which results in minimal distortion of an output voltage and power quality improvement. In the SLMLI, the productive output voltage and performance factors such as harmonic minimum distortion values, are analysed. The contrast obtained when comparing hardware and simulation is the value of 4.35% THD in the simulation model and 12.90% THD in the hardware model.

The validity of the simulated results is tested by a single-phase 15-level firefly assist FPGA prototype model with the effect of less switching stress and minimal electromagnetic interference. In the simulation and hardware implementation, the plus or minus ten voltage deviation from R and RLE loads is due to the variation of load and the absence of filter components, which reduce the cost of the inverter circuit. The total harmonic distortion values in RL and RLE load conditions were almost the same. The reactive power is developed 65.38 VAR effectively in RL load condition due to the power consumed by inductance and the main capacitor bank unit, in order to keep the system to be balanced. The symmetrical SLMLI notion will soon to be a great choice for power electronic frameworks, particularly for solar PV applications.

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