Power efficient digital circuits for ECG front end data acquisition mobile system

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Abstract: The electrical motion of the heart is characterised by the ECG signal. ECG elucidation can be used to detect the heart syndrome. This technology has an efficient diagnostic tool, due to the high regard of portable electronic products, low power system has fascinated more consideration in recent years. This work presents digital ECG data acquisition system to diminish the power consumption. In the proposed work, analogue block is not used, they convert the input voltage into a digital code by delay lines. This digital architecture is capable of operating with a low supply voltage such as 0.3 V and 0.1 V. In this architecture, analogue blocks such as low-noise amplifier (LNA) and filters are not used. A digital feedback loop is employed to cancel the impact of the dc offset on the circuit, which eliminates the requirements for coupling capacitors. The circuit is implemented in 130 nm and 65 nm CMOS process. The simulation results illustrate that the front-end circuit of digital architecture for 130 nm consumes 18.9 pW and 65 nm consumes 109 pW of power.

Keywords: electrocardiogram; ECG; mobile monitoring; digital; amplification; analogue; acquisition; delay; offset.

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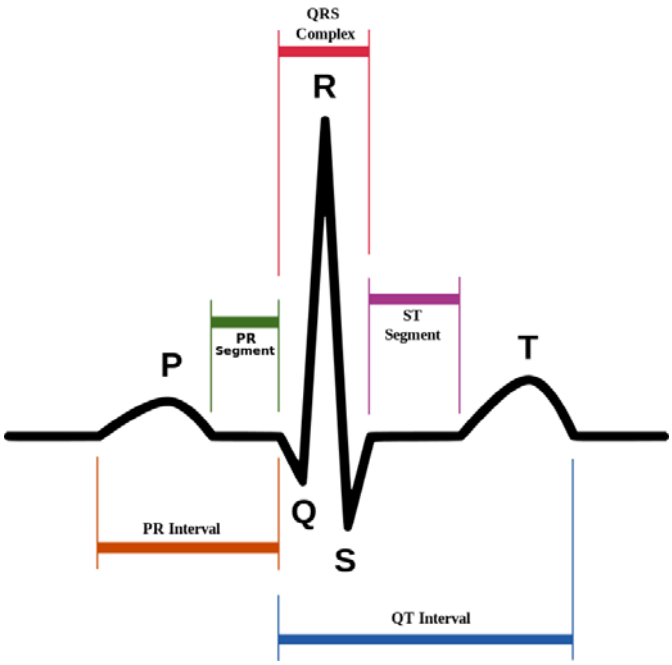
1 Introduction

Data acquisition is the process of sampling signals that quantify real world physical conditions and converting the ensuing samples into digital numeric values that can be manipulated by a computer. Data acquisition systems, truncated by the acronyms DAS, usually alter the analogue waveforms into the digital values for processing. Electrocardiogram (ECG) is a depictive recording of electrical activity of the heart over time. It is recurrently recognised by the biological signal and among non-invasive method; it is generally used for analysis of some diseases by construing the signal. Cardiovascular diseases and its abnormalities change the ECG wave shape; each portion of the ECG waveform carries information that is pertinent to the clinician in arriving at a proper diagnosis is shown in Figure 1.

The ECG sensor is to acquire the effect of the human body heart sounds ECG signal, translates into electrical signal which is generally unsteady, accompanied by noise and it should be based on the modulation of the circuit filter and amplification. A signal acquisition system is static hardware and software instrumentation, noise or other distinctiveness filtering and trade out for the evocation of information (Kim et al., 2013).

It is used to extract several characteristic considerations. At present, biomedical signal processing have been towards quantitative or the objective analysis of physiological systems and phenomena via signal analysis sector.

Figure 1 ECG waveform (see online version for colours)



ECG analysis concerns resting ECG elucidation, stress testing, peripatetic monitoring or intensive concern monitoring, which forms a essential set of algorithms that conditions the signal with respect to different types of noise and artefacts which helps to sense heartbeats, haul out fundamental ECG measurements of wave amplitudes and durations and compress the data for an resourceful storage or transmission. In all these applications, the biosignal is first preconditioned and converted to the respective digital code. A digital signal processor then processes the digital data for monitoring or diagnosis applications. Biomedical signal acquisition systems generally consist of a low-noise amplifier (LNA) and an analogue-to-digital converter (ADC) is the mostly commonly used analogue devices. Normally, these devices drain more amounts of power and area. Digital systems cooperate a significant role in today's life. They have significant applications in virtually all fields of human activity and have a global influence on the performance of society. Digital portray electronic technology that generates, stores and processes data in stipulations of two states: positive and non-positive. Positive is articulated or represented by the number 1 and the non-positive by the number 0. Thus, statistics transmitted or stored with digital technology is asserted as a string of 0's and 1's. Each of these state digits is invoked as a bit. In a digital system, a more rigorous representation of a signal can be obtained by using more binary digits to represent it. Although this requires additional digital circuits to process the signals, each digit is directed by the same kind of hardware, proceeding in an easily scalable system. Biomedical signal acquisition systems

(Zare and Maymandi-Nejad, 2015) usually consist of a LNA, a band-pass filter, an analogue model and hold, also an ADC. Typically, analogue block consume more amount of power and area compared to the digital architecture. This digitally improved approach can facilitate to increase the extensibility of the system in removing the unwanted interferences. With the enhancement of CMOS technology, the supply voltage is being condensed, which deflates the voltage headroom for analogue block of an IC (Sivaranjani and Sasikala, 2017). The technology scaling heads to the lower power consumption and higher performance in digital circuits. The constraints such as signal-to-noise ratio (SNR), dynamic range and gain of the analogue design of an IC are depressingly impacted. The power utilisation in a signal processing system is reiteratively determined by dynamic range constraints. The dynamic range is a measure of the ratio between the largest signal that can be handled by the system without an eloquent distortion and the minimum detectable signal set by the input-referred noise. Therefore, it is covetable to find new architectures in which more digital blocks are employed. However, there are other concerns that should be consigned before moving close to the fully digital performance. Two of these issues are as follows (Tsai et al., 2012).

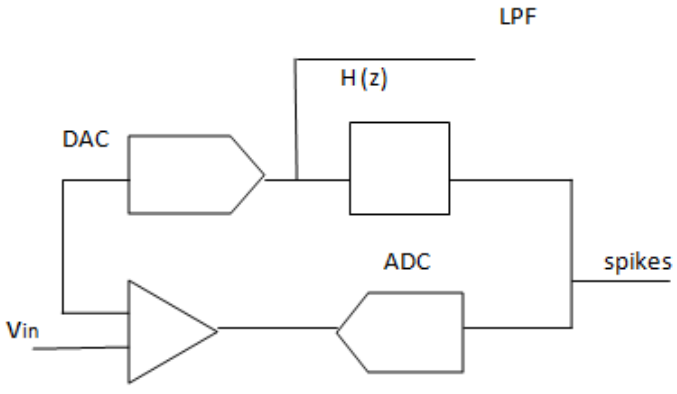
1 detaching the DC offset voltage of electrodes without passive elements

2 providing a resolution for anti-aliasing filter.

The block diagram of the system designed in Shiu et al. (2013) is shown in Figure 2. In this circuit, several of the functions that are normally implemented by analogue blocks are performed by digital circuits. Using this digitally improved approach can help to amplify the flexibility of the system in removing an unwanted noise. Eliminating the interferences at the input of the system, before extensive gain is applied, this can relax the dynamic range requirements and reduced the supply voltage. This can guide to reduce the overall power consumption and area of the system (Muller et al., 2012).

This can be achieved by using mixed signal feedback and the digital circuits. Hence, the use of digital techniques in the implementation these systems that which can helps to get a better performance and better compatibility with digital CMOS technology.

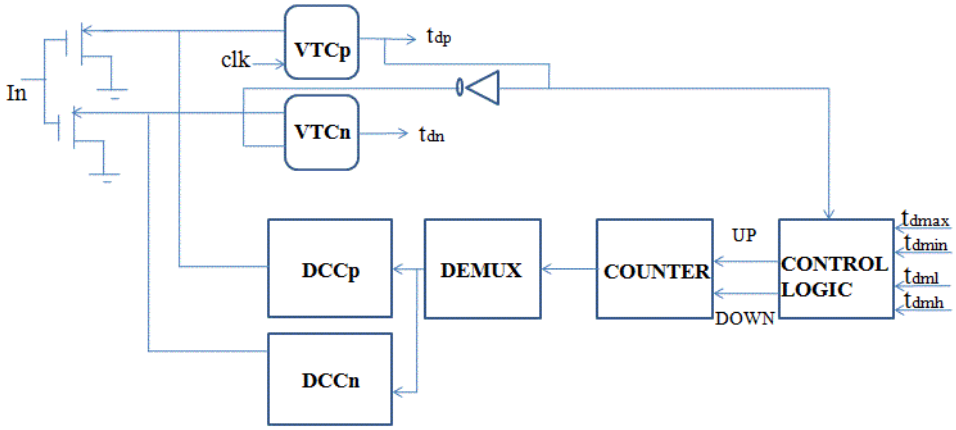
Figure 2 Mixed signal feedback architecture



2 Digital front end architecture

A new power-efficient ECG acquisition system that uses a fully digital architecture is proposed. In the system, active electrode, DCC, Demux and counter is implemented in the 130 nm and 65 nm CMOS technology to evaluate its performance. The supply voltage is 0.3 V and 0.1V and the circuits are designed to operate in the sub-threshold region to reduce the power consumption (Harpe et al., 2015). Each block of the structure and its propose challenges is discussed in the following sections. The biosignal is generated from the active electrode is directly given to the two VTC blocks are used is shown in the Figure 3. These blocks are in charge of generating a current that depends on the 32-bit digital number (SW0 to SW31).

Figure 3 Digital front end architecture (see online version for colours)



The ECG signal acquisition system should be capable of rejecting the dc polarisation voltage of the bio-potential electrodes, appearing as a dc offset at the input. This requires a high-pass filter (HPF) with a cutoff frequency < 1 Hz. This filter requires large capacitors and on-chip implementation of such a filter is not efficient in terms of area. The impact of the offset is removed. This is achieved by a digital feedback loop and allows the circuit to take the value of the offset to the digital output.

2.1 Active electrode

An active electrode is an electrode, in which a few active elements are used to reduce the power line interference. Figure 4 demonstrates two dissimilar two-wired active electrodes for comparison. The circuit in Figure 4(a) uses an op-amp, while the one in Figure 4(b) is implemented using a single transistor. In Tsai et al. (2012), important parameters of such electrodes, such as offset, noise, gain and output resistance are compared. It is shown in Tsai et al. (2012) that the circuit in Figure 4(b) has a superior performance in terms of noise, common mode rejection ratio (CMRR) and power consumption compared with the circuit of Figure 4(a). Since, in ECG applications, the mainly significant limiting factor is the input noise of the system, we have utilised the active electrode with a single MOS transistor.

Figure 4 Active electrode with either (a) an op-amp or (b) a MOS transistor

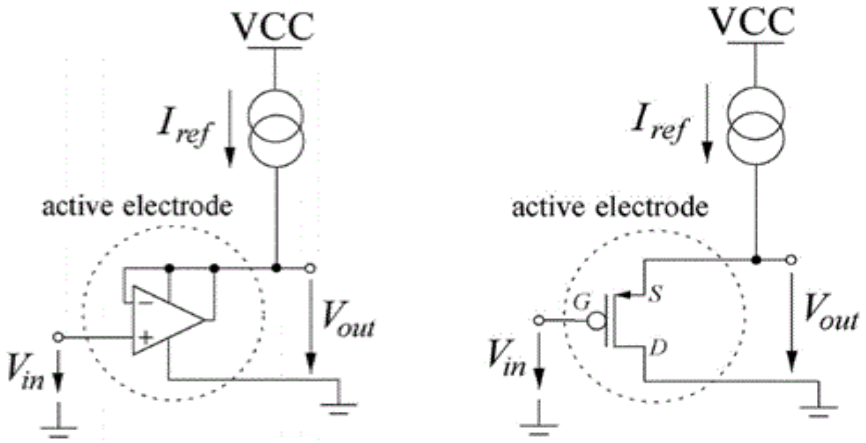
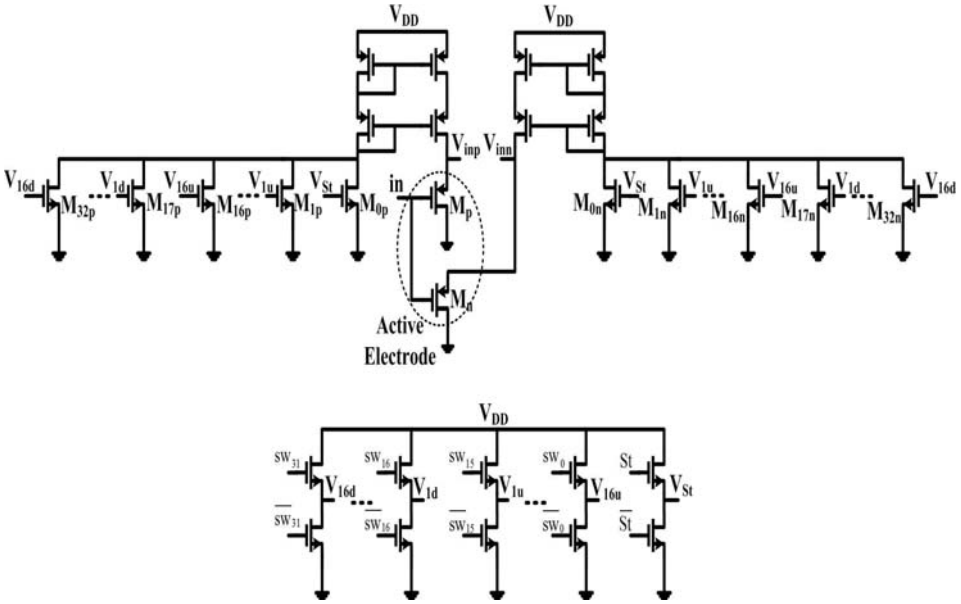


Figure 5 Structure of the current DCC



2.2 Digital to current converter

In the fully digital ECG front-end architecture of Figure 5 shows two DCC blocks are exploited. These blocks are in charge of making a current that depends on the 32-bit digital number (SW0 to SW31) at the output of the Demultiplexer. The DCC circuit, in which generates the gate voltages required for the reference current generator in the upper circuit. The currents fabricated by transistors M0*p* to M32*p* and M0*n* to M32*n* pass

through transistors M*p* and M*n* to generate the two voltages *V*inp and *V*inn (Shih et al., 2014). These voltages are then pertained to the VTC*p* and VTC*n* blocks. The DCC generates a current which is proportional to its digital input and decreases/increases the input voltage of the VTC*p* and VTC*n*, each LSB of the DCC corresponds to more or less 3 mV and this voltage is added to/subtracted from the system in every step.

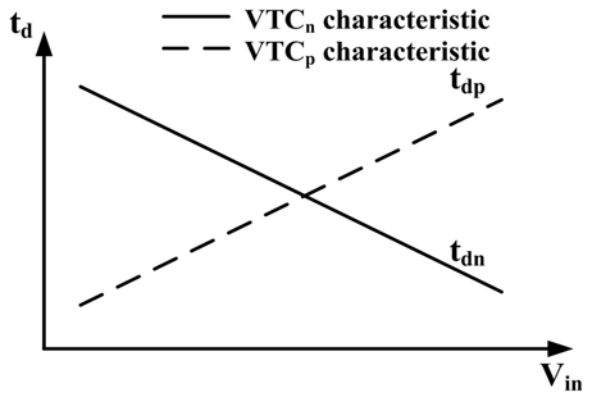
To recognise the performance of the DCC, imagine that the offset at the input increases (decreases) dominated to a rise (fall) in *V*inp and *V*inn (Tu and Lin, 2014). Since a result, the delay of the VTC*p* block amplifies (decreases) and that the VTC*n* decreases (increases). As can be seen, at the commencement, the offset cancellation circuit is interim and setting the output of the DCCs and behind this transition time the output signal is reliable.

2.3 Voltage to time converter

In this digital implementation, the analogue input voltage is converted to a measurable time via a VTC at the first stage (Tsai et al., 2012). The signal information is now in the delay of clock signal (CLK). The VTC should be planned in such a way that the small amplitude of the input voltage generates a large delay, linearly. In sort to have the time-domain amplification and acceptable SNR, we have employed 15 stages of positive VTC (VTC*p*) and 15 stages of negative VTC (VTC*n*). The delays against input voltage of VTC*p* and VTC*n* are shown in Figure 6. As the input voltage becomes superior, the delay of VTC*p* increases, while the delay of VTC*n* decreases. The cascaded stages of VTCs form delay-line structures in the system to adhere delay effects.

A major benefit of the delay-line-based structure lies in its all-digital implementation (Sivaranjani and Sasikala, 2016).

Figure 6 VTC*n* and VTC*p* characteristics



For example, the first VTC integrates the signal from the rising edge of the clock to the time equal to the delay of this VTC. The subsequent VTC integrates the signal from the rising edge of the output of the first VTC over a time period determined by its delay. This occurs for all the VTCs in the chain. The sum of these incorporation periods is equal to the clock period. Hence, the incorporation over this time window can be represented by as:

$$Y(T_s, t) = 1/T_s \int (V_{in}(\tau) d\tau) \tag{1}$$

Therefore, its impulse response is a rectangular pulse in the variety of [0, *Ts*]

$$\delta(\tau)d\tau = u(t) - u(t - Ts) \tag{2}$$

Hence, its frequency response is a sinc function

$$H(j\omega) = 2\sin\left((Ts/2)\omega\right)/\omega Ts \tag{3}$$

In this way, the moving normal filtering is embedded in the MA-VTC, preventing aliasing of the wideband noise (Bohorquez et al., 2011).

2.4 Clock frequency and signal recovery

VTC*p* and VTC*n* blocks are designed in such a way that the absolute slopes of their characteristic curves are equal. Hence, for any input voltage, we can mark

$$tdp + tdn = t_{tot} = \text{Constant} \tag{4}$$

The delay time *tdp* (or *tdn*) of a VTC gate is believed to be a linear function of its input voltage and is given by

$$tdp = \alpha V\text{inp} + \beta 1 \tag{5}$$

$$tdn = \alpha V\text{inn} + \beta 2 \tag{6}$$

where *V*inp and *V*inn are the input voltage during the time interval that the clock pulse passes through VTC*p* and VTC*n*, correspondingly. In count, α, β1 and β2 are constants. The clock period, *T*clk, must be special such that for the maximum variation of the input *tdn* is not zero and is forever measurable. Therefore, the clock period should be slightly extra than t_{tot}. Hence

$$T\text{CLK} \geq tdp + tdn = \alpha(V\text{inp} - V\text{inn}) + \beta 1 + \beta 2 \tag{7}$$

The outputs of the digital front end are *tdP* and *tdn*. These delays are transformed to two digital numbers (*DP* and *DN*) by two TDCs. The digital number matching to the input voltage, *D*in, can be achieved from

$$D\text{in} = Dp - Dn / 2D\alpha + D\beta 2 - D\beta 1 / 2D\alpha \tag{8}$$

where Dα, Dβ1, also Dβ2 are digital numbers of α, β1 and β2, respectively.

2.5 Control logic

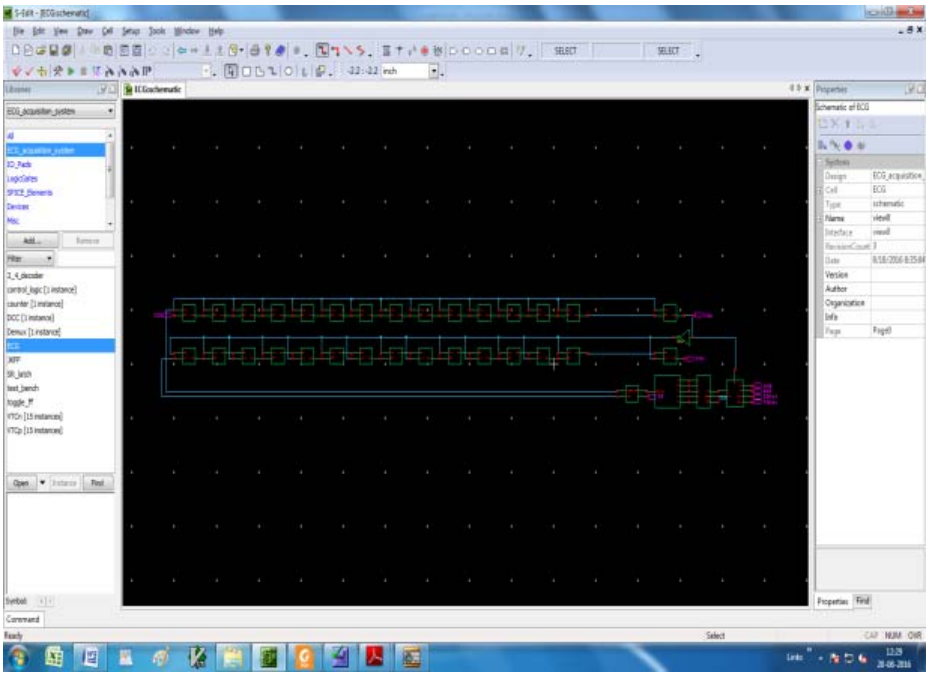
It is composed of TCs, AND and OR gates and set-reset (SR) latches. To detect the offset, the control logic should compare *tdp* with four predefined delays (*td*max, *td*min, *tdml* and *tdmh*). Note that in an analogue front end, for identifying the offset voltage, an analogue voltage comparator should be employed. In our design, the offset is sensed by TCs, which are implemented by D flip-flops and are more power and area efficient compared with the analogue voltage comparators. The productions of the control logic

circuit are the UP and DOWN signals, which manage the up/down counter in the offset termination block. The counter in our design is executed by NAND gates and jk flip-flops.

3 Simulation results

Figure 7 shows that the overall ECG schematic diagram is designed using two technologies 130 nm and 65 nm with corresponding supply voltage 0.3 and 0.1 which consists of simply VTC, DCC, Demux, control logic and counter. Here, the input is given to the gate of the NMOS and PMOS of the active electrode is connected to the DCC.

Figure 7 Schematic diagram of ECG (see online version for colours)



The input voltage given in this block is 200 mv and the output is nearly 20 mv. The biosignal coming from the active electrode initially contain some unwanted noise, VTC block cancel out the offset voltage is shown in Figure 8.

Table 1 Result analysis

	Existing system	*Proposed system*	
Technology	0.18 µm	0.13 µm	0.65 µm
Supply voltage	0.5 V	0.3 V	0.1 v
Power consumption	274 nW	18.0 pW	109 pW

The input voltage given in this block is 100 mv and the output is nearly 12.5 mv. The biosignal coming from the active electrode is given to VTC block to cancel out the offset voltage shown in Figure 9.

Figure 8 Output waveform of 130 nm (see online version for colours)

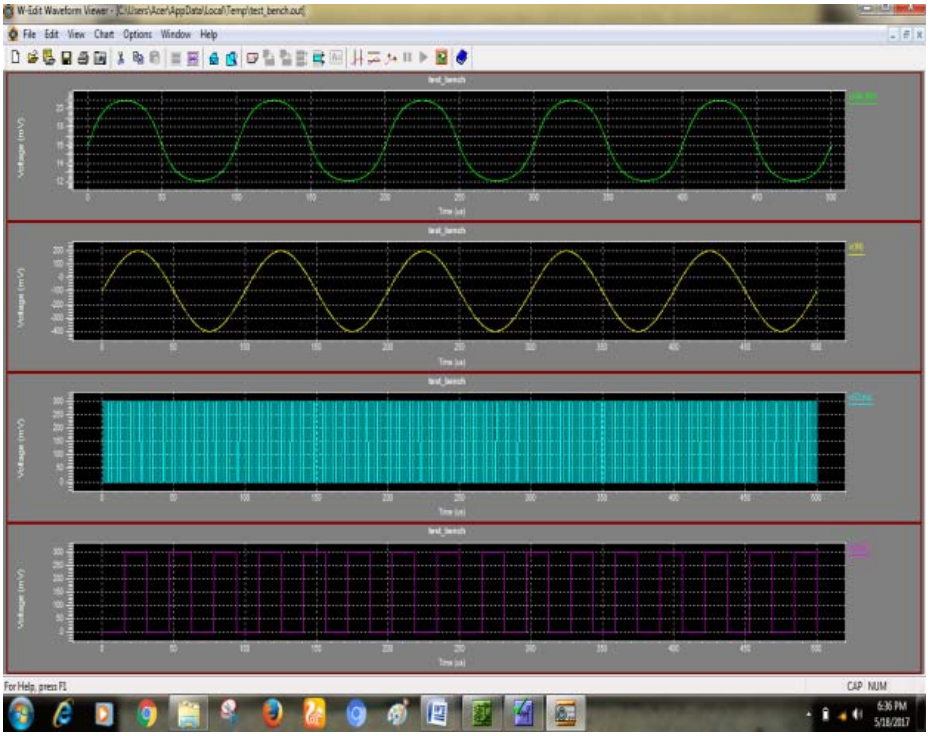
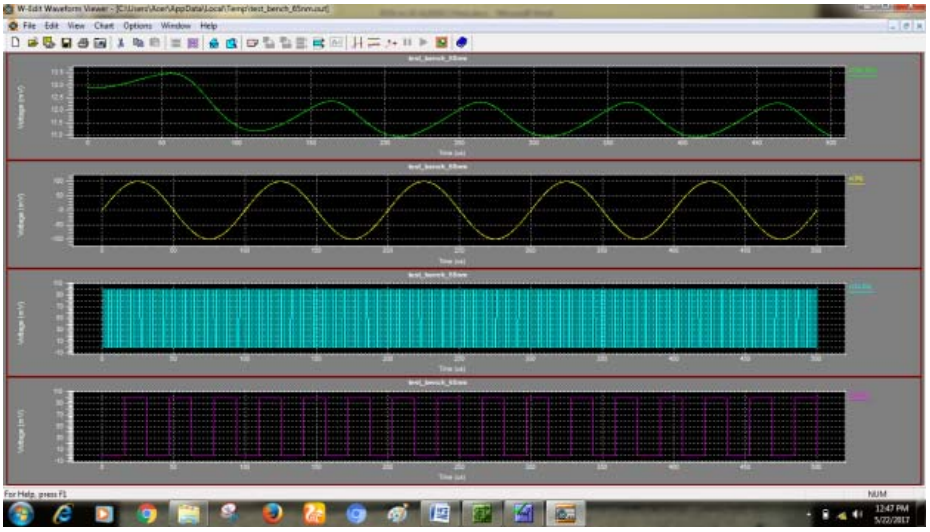


Figure 9 Output waveform of 65 nm (see online version for colours)



4 Conclusions

In the expectation of the future dominance of digital CMOS technology, a fully digital front-end construction for an ECG acquisition system was designed. In this system, active electrode, DCC, control logic and VTC circuits were performed. The system has low power consumption, reduced delay time and fewer complexities. This digital architecture is simulated in 130 nm CMOS technology at 0.3 V supply voltage consumes 18 pW. The same architecture is simulated in 65 nm CMOS technology at 0.1 V supply voltage consumes 109 pW. The digital architecture can be modified to accept an offset voltage larger than ±300 mV. In order to do this, the resolution of the DCC circuit and de-multiplexer should be increased to eight bits. A new offset cancellation technique is used, which reduces the 50 mV offset voltage to < 5 mV and makes it tolerable for the system. A moving average mechanism embedded into the VTC of the front end eliminates the need for anti-aliasing filter.

Acknowledgements

All authors contributed equally.

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