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An efficient Architecture for Barrel Distortion Correction in Surveillance camera images

A Sathya and D Sasikala

Vivekanandha College of Engineering for Women, Namakkal, India.

E-mail :Sathyatamil03@gmail.com and adhivasan@gmail.com

Abstract. Barrel Distortion Correction algorithm has been widely used to eliminate the distorted image in the wide angle camera. The distortion occurred due to lens dislocation in the camera. Nowadays, various image Processing algorithm are developed to correct this distortion. In this Proposed work Design of an efficient Architecture for correcting this distortion. The proposed architecture consist of Backward Mapping and linear interpolation units. FPGA family Devices like Cyclone II, Cyclone III, Stratix II and Stratix III are used for verifying the Parameters such as LUT, Power and Time can be measured and compared. The Backward Mapping is done here with linear interpolation. The power consumption and time taken for correcting the distortion is reduced.

Key Terms. Wide angle camera, Barrel Distortion Correction, Backward Mapping, FPGA, Linear interpolation.

1. Introduction

In industrial imaging system, wide angle camera is widely used. This imaging system is very useful in video inspection systems, automotive black boxes, radars imaging, and medical applications. So there is a possible of occurring distortion in images captured by the wide angle cameras. This type of distortion is called as Barrel Distortion. This distortion can be attained because of expected optical aberrations. For certain application, this is being a serious issue. This type of distortion is banned by using the lens with their physical characteristics is exact to the ideal. Then only the distortion is not affected in the images. But this is not sufficient in real time for the utilization of low cost system due to high expense of lens. So digital signal processing algorithm has emerged to correct the barrel distortion [1].

In recent decades, different types of methods developed to correct the Barrel distortion. Some of the important methods are follows: [2] (Min Qi et al 2012) presented a novel and suitable method for BDC in images. This method is based on the Polar Coordinate Transformation. The present struggles in correcting the Barrel distortion are overcome by an improvised Polar Coordinate Transformation. [3] (Hui-Sung Jeong and Tae-Hwan Kim 2015) detailed a method for correcting the Barrel Distortion with hardware architecture. The distortion correction algorithm is combined with the color demosaicking to perform the elimination of distortion. [4] Sam Van et al 2015 designed a novel method for correcting the distortion in GPU which affects the required manipulation to many parallel stream processors.The projected technique is not restricted to affine lens distortions but permits for the correction of discretionary geometric image distortion artifacts through individual element resampling at show rates of over thirty frames per second for completely processed footage (1024 × 768 pixels).

The correction algorithm is associated with the memory presented by [5 Won-Tae Kim et al 2014] which utilizes the locality of the memory access. It uses the 17.2K logic gates with correction speed of 205 Mpixels/s. Junhee Park et al [6] implemented an algorithm for defining on ideal accurate coordinates. Computation time and high accuracy can be obtained.


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This paper is organized as follows. Section II describes Barrel Distortion Correction technique, Section III describes the 15 stage backward mapping and color interpolation unit. Experimental results are described in Section IV and conclusion is described in Section V.

2. Barrel Distortion Technique

2.1.Forward Mapping

Let DIS and CIS represent the distorted and corrected image spaces [7 Chen et al 2009]. (x_c',y_c') is denoted as the distortion center in DIS. (x_c,y_c) is represented as the correction center in CIS, (x',y') represents the Cartesian and the polar coordinates of a pixel is denoted by (p',Θ') where p' is the distance and Θ'is the angle from the distortion center (xc',yc') to (x',y') are given by equations (1) and (2).

$$\rho' = \sqrt{(x' - x_c') + (y' - y_c')} \tag{1}$$

$$\Theta' = \arctan \frac{(y' - y_c')}{(x' - x_c')} \tag{2}$$

The new location of same pixel in CIS is (x,y). The distance p and the angle Θ from the correction center (x_c,y_c) to (x,y) are given by equations (3) and (4).

$$\rho = \sqrt{(x - x_c) + (y - y_c)} \tag{3}$$

$$\Theta = \arctan\left(\frac{(y - y_c)}{(x - x_c)}\right) \tag{4}$$

Figure 1 shows the block diagram of the BDC algorithm. Barrel distortion can be corrected by three important operations: first one is forward mapping of all the pixels, second is back mapping of all vacant pixels, and finallymeasuring the intensities for all vacant pixels by linear interpolation [8Hau T. Ngo et al 2005].

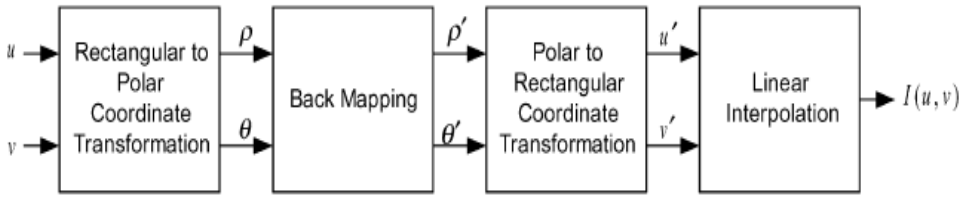


Figure 1. Block Diagram of the BDC algorithm

2.2.,*Back Mapping*

After the pixel arrangement from DIS into CIS, the pixel vacancy can be created and the vacancy intensity values are computed. This vacant pixel (x,y) has a new location of (x',y') in DIS. [9 K. V. Asari et al 1999] implemented the back-mapping procedure by polynomial of degree is expressed by a polynomial in equation (5).

$$\rho' = \sum_{n=1}^{N} b_n \rho^n$$
$$\Theta' = \Theta \tag{5}$$

where are the b_n back-mapping coefficients. Expansion process is used to give dot locations sets in DIS

and their parallel dot locations in CIS which are mentioned in the forward mapping section. For a particular dotset, a nonlinear regression analysis is applied for least-squares estimation. This process is done to extract the back-mapping coefficients b_n' which plots the dot locations in CIS to resultant dot locations in DIS. The pixel location (x',y') corresponding to the updated values p' and Θ' is shown in equation (6).

$$x' = x_c' + \rho' \cos\Theta'$$
$$y' = y_c' + \rho' \sin\Theta' \quad (6)$$

2.3.Linear Interpolation

The pixel location (x',y') resultedin the back-mappingprocedure is not be an integer location. The pixel intensity value of four neighboring pixels of (x',y') are used to compute the pixel intensity value of this location by linearly interpolating. A and B are integer parts of the coordinate values. The values of these coordinates is expressed in equation (7).

$$A = |x'|$$
$$B = |y'| \quad (7)$$

The partial parts of the coordinate values represented by A'and B' is given by equation (8).

$$A' = x' - A$$
$$B' = y' - B \quad (8)$$

3.Proposed Methodology

The Barrel Distortion Correction architecture is shown in Figure 2. When the beginning signal is enabled, the circuit can output the intensity price of the primary constituent when twenty one clock cycles. Then, it will method one constituent in CIS per clock cycle. Our style consists of 4 main modules: mapping unit, memory bank, linear interpolation unit and controller. The elaborate circuits of mapping and linear interpolation units square measure delineated as follows.

The mapping unit performs the calculation of (x',y'). The memory bank consists of 4 duplicated RAMs accustomed offer the intensity values of the four neighboring pixels around (x',y') at the same time. the scale of every RAM is adequate that of input image that is about as 1024 X 1024 bytes within the current implementation. The interpolation unit linearly interpolates the ultimate intensity price. The managementler provides the control signals of every state to different units and handles the total correction procedure.

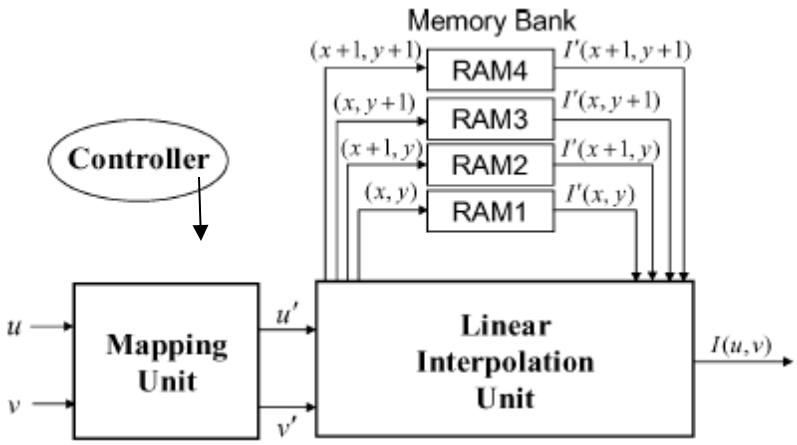


Figure2.Barrel Distortion Correction architecture

3.1.ProposedBackward mapping unit

The backward mapping method entails calculation of the mapping polynomial to get the dimensions issue of the picture element location. within the planned design, the backward mapping is performed with fifteen stages. for every picture element (x,y) in CIS, the mapping unit performs the operations required (x',y') to calculate (from state S1 to state S11 in Figure. 3). Most multipliers and adders square measure complete with 24-bit breadth as adopted in [8]. It's found that the propagation delay of a 24-bit multiplier factor is kind of long. Hence, we have a tendency to adopt the 24-bit two-stage pipelined multiplier factor within the style to urge higher pipeline programming. Figure. 3 show the pipelined design of the mapping unit. Within the figure, the shadowy rectangles square measure registers, the ellipses marked with square measure two-stage pipelined multipliers, and therefore the variables square measure a twin of those shown in Figure. 3.

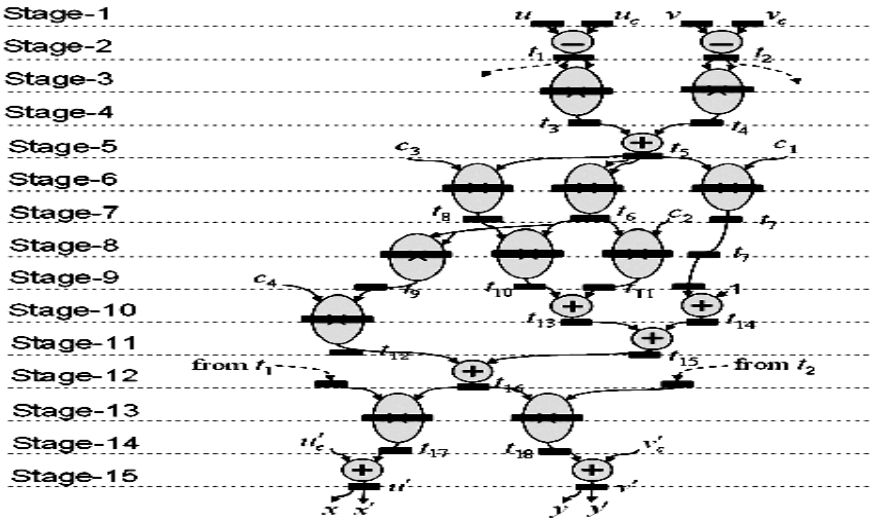


Figure3. Proposed architecture for Backward mapping unit

3.2.*Proposed Linear Interpolation Unit*

The linear interpolation unit obtains the intensity values of the four neighboring pixels around (x',y') and measures the final intensity value I(x,y). Figure. 4 shows the proposed pipelined design of the linear interpolation unit.

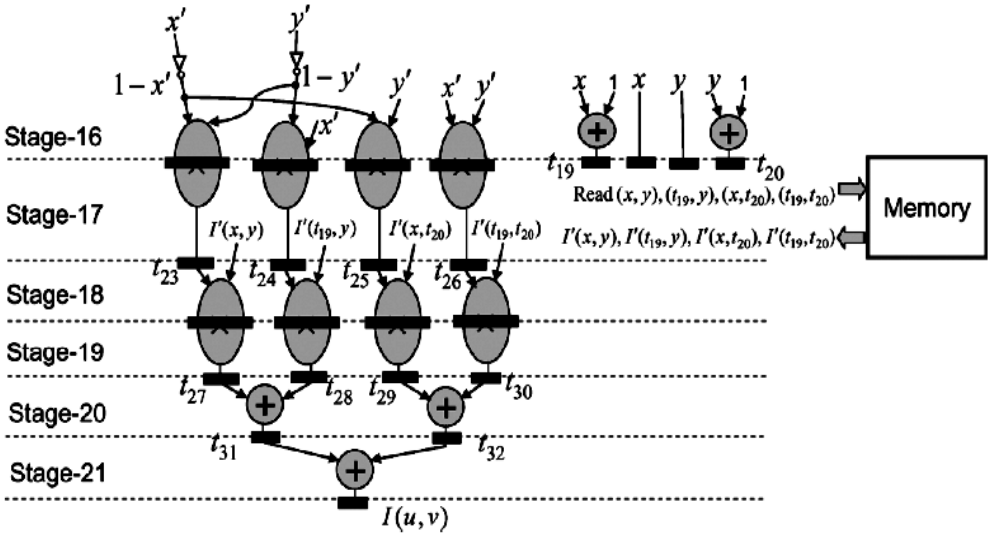


Figure 4. Proposed design for linear interpolation unit.

The Linear Interpolation unit performs the operations required to analyze I(x,y) (from state S12 to state S17 in Figure. 3). At each clock cycle, four neighboring intensities area unit accessed at the same time and one output intensity price is generated consequently.

4.Results of Proposed Method

The VLSI Architecture of the proposed method was Designed by usingQuartus II as the supporting platform. The VHDL code for mapping unit was analyzed and synthesized in FPGA devices like Cyclone II, Cyclone III, Stratix II and Stratix III. The corresponding LUT, power and timing analysis are measured and tabulated in Table 1. The RTL view of these units is shown in Figure. 5.

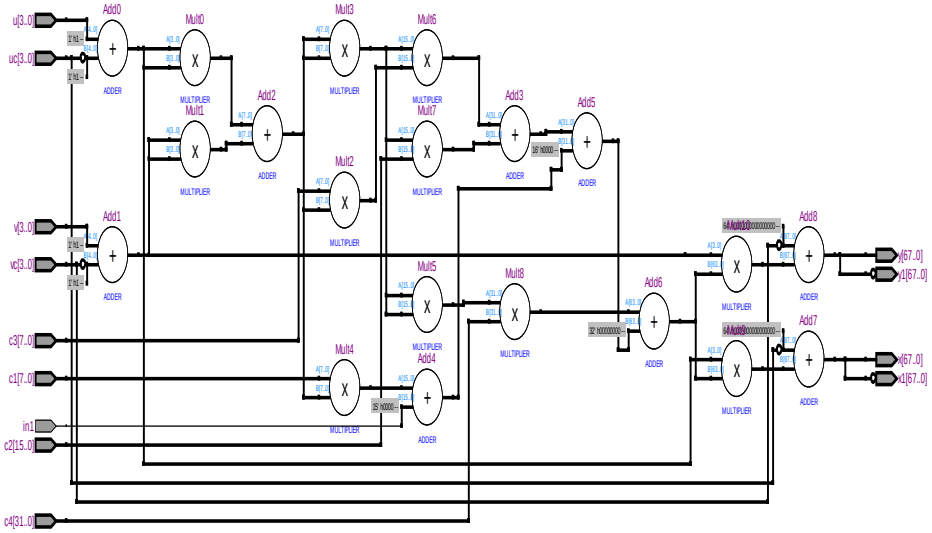


Figure 5. RTL View of the backward mapping unit

Table 1. Parameter analysis of Proposed Backward mapping unit

Parameter	Cyclone II	Cyclone III	Stratix II	Stratix III
LUT	959	535	1056	320
Power (uW)	9684.85	3607.80	4992.61	1550.20
Time (pS)	54.747	48.601	69.543	43.784

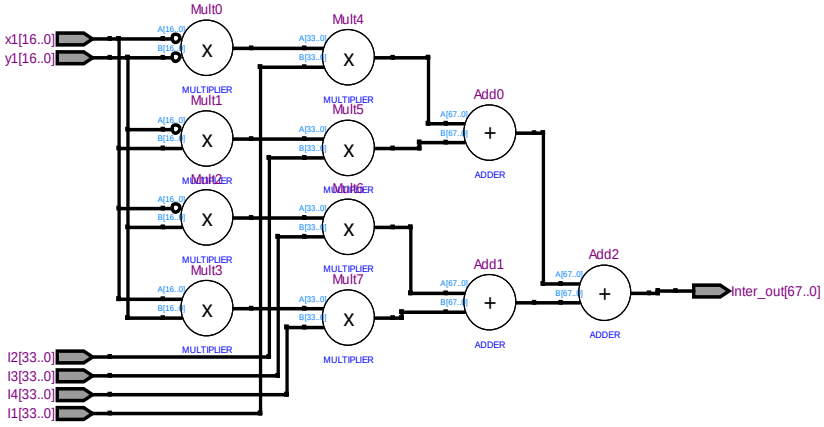


Figure 6. RTL View of Linear Interpolation Unit

Table 2. Table parameter analysis of Proposed Linear Interpolation unit

Parameter	**Cyclone II**	**Cyclone III**	**Stratix II**	**Stratix III**
LUT	3011	544	238	208
Power (uW)	5914.86	705.87	1142.05	929.94
Time (pS)	35.742	28.143	26.444	28.887

The RTL view of the linear interpolation unit is shown in Figure 6. Table 2 and Table 3 show the parameter analysis of both linear interpolation unit and proposed BDC algorithm. The BDC algorithm is implemented in different FPGA devices as mentioned above. Compared to performance analysis to each other, stratix III FPGA device family is efficient in terms of LUT, power and time. It was clearly shown in Figure 7.

Table 3. Table parameter analysis of Proposed BDC algorithm

Parameter	Cyclone II	Cyclone III	Stratix II	Stratix III
LUT	2811	1505	377	377
Power (uW)	19835.70	10180.79	4917.24	3920.71
Time (pS)	72.146	63.406	52.136	53.847

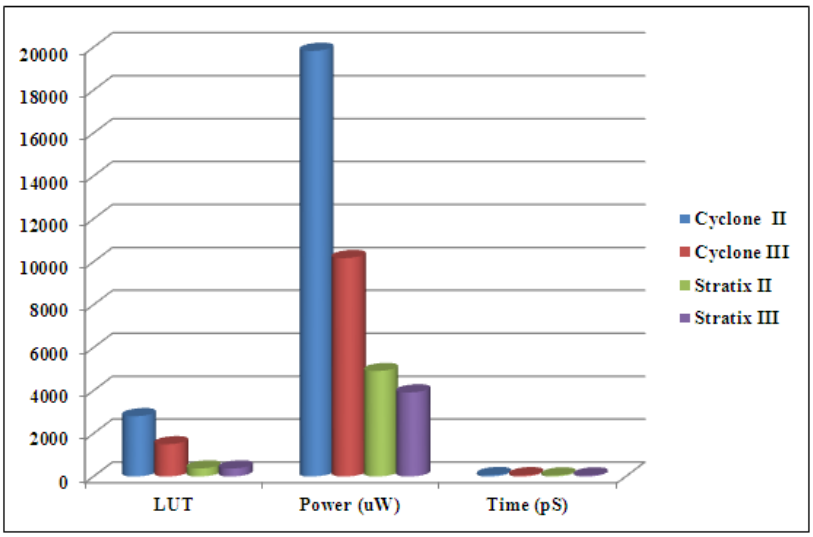


Figure 7. Performance comparison of Proposed BDC algorithm in different FPGA device family

5.Conclusion

The Proposed Architecture consist of two main blocks one is Backward Mapping unit another one is linear interpolation unit by Designing and implementing these two process. The barrel distortion present in the image can be eliminated. The removal of distortion in image is a Digital Process, VHDL language is used for correcting the distortion. The proposed work is done in 90 and 65 nm CMOS Technology. As a result the, the proposed BDC algorithm is well suited in Stratix III FPGA device families compared to Cyclone II, Cyclone III and Stratix II. From the corrected image many useful information can be identified.

6. Future Scope

An Architecture is designed here with two different nm CMOS Technology for correcting the Barrel Distortion in wide angle camera images. In the Future the Architecture may be implemented in FPGA Devices, Further reduction in power consumption, Time delay may be done.

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