PERFORMANCE ANALYSIS OF SINGLE-WALLED CARBON NANOTUBE AND MULTI-WALLED CARBON NANOTUBE IN 32nm TECHNOLOGY FOR ON-CHIP INTERCONNECT APPLICATIONS

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Abstract- The semiconductor industry is facing a crucial problem in the interconnect section when IC is scaled down below 32nm technology. Scaling increases the number of devices per unit area, which in turn increases the performance of the transistor resulting in the overall increase of performance per unit area. But there is a decrease in the performance of interconnect especially in that of global interconnect. The reduction in the cross section of copper interconnects in accordance with technology scaling, increases the resistivity due to size effects. This increase in resistivity affects performance, namely delay and current carrying capability of copper interconnect. Carbon nanotube is proposed as the replacement for copper to alleviate the bottleneck in all levels of interconnects because it has high mean free path and ballistic transport. The performance evaluation of both single-walled carbon nanotube and multi-walled carbon nanotube interconnect delay is carried out and the results are compared with that of the copper interconnects. Both the CNTs and copper interconnects are examined thoroughly with the help of HSPICE simulation using its transmission line model. Comparison shows that MWCNT is the most promising candidate for local, intermediate and global levels of interconnects.

Index Terms- Copper (Cu), Carbon Nanotube (CNT), Single-walled CNT (SWCNT), Double walled CNT (DWCNT), Multi –walled CNT (MWCNT), On-chip interconnect, 32nm technology.

I. INTRODUCTION

The rapid growth of the VLSI technology is mainly due to the constant reduction of the feature size of VLSI devices. Once the active devices and regions are fabricated they must be electrically connected to each other to make circuits. They must also be connected to the outside world through their inputs and outputs on bonding pads [10]. Making these connections is the job of contacts, vias and interconnects. Interconnect can be classified as local, intermediate and global [21]. The geometry of interconnect is as shown in Fig 1(a). As the technology scales down, transistor performance improves and the interconnect becomes an issue in multicore processors [22]. In early 90's, the shrinking of wire dimensions caused Al interconnects to suffer from high electromigration resistance. Hence, Copper was considered as an alternative for Al interconnects due to its low resistivity. In Nanometer region, Cu interconnects face serious problems such as electromigration, surface and grain-boundary scattering of electrons. This is due to the wire dimension reduction in nanometer scale and it leads to increase in resistivity [2]. As a result, copper interconnects have increasing performance degradation, which will compels the researchers to find an alternate interconnect material to improve future IC performance. According to International technology roadmap (ITRS) 2011 [23], Carbon nano materials like Carbon Nanotube (CNT), Graphene Nanoribbon (GNR), carbon nanowires, optical interconnects etc have emerged as the promising candidates for future VLSI interconnects [12-20].

The excellent electrical, mechanical, thermal properties and high current capacity ~10^{10}A/cm^2 makes CNT, the suitable successor of copper interconnect. The structure of CNT is shown in Fig 1(b).It has long mean free path which allows the ballistic transport of electrons over a long distance offering low resistance. Carbon nanotubes (CNTs) are graphene sheets rolled up into cylinders with diameter in the order of nanometers [2]. Depending on the direction in which CNTs are rolled up (Chirality), they acquire either metallic (a_1=a_2) or semi-conducting (a_1=0 or a_2=0) properties as shown in Fig1 (c) [11]. Armchair structure exhibits metallic characters whereas zigzag structure exhibits semiconductive characters.

In paper [9] the Cu and SWCNT have been compared, in these comparisons SWCNT has been proposed as better interconnect for future generations. In this paper, the Copper, Single-walled carbon nanotube and Multi-walled carbon nanotube interconnects are compared by their circuit models in 32nm technology. From the comparisons, the MWCNT is shown to be suitable upcoming interconnect material for all level of interconnects due to its low delay and high bandwidth.

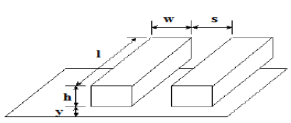
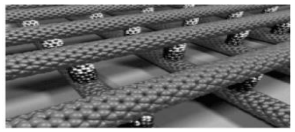


Fig.1.(a)Interconnect geometry


(b) Structure of CNT

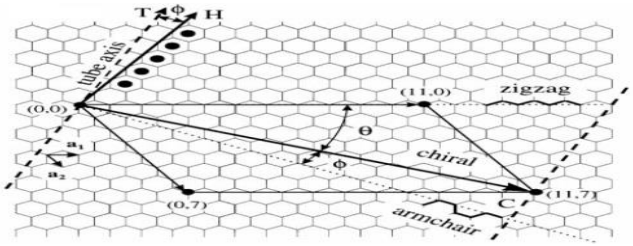


Fig.1. (c) Chiral vector for CNT characterization

For interconnect applications, CNT should exhibit metallic character. Classification of CNT is based on the number of tubes rolled up: SWCNT, MWCNT.

SWCNT consists of a single layer of graphene sheet as shown in Fig 2(a) flawlessly wrapped into a cylindrical tube, with diameters ranging between 0.7 to 10nm [2].

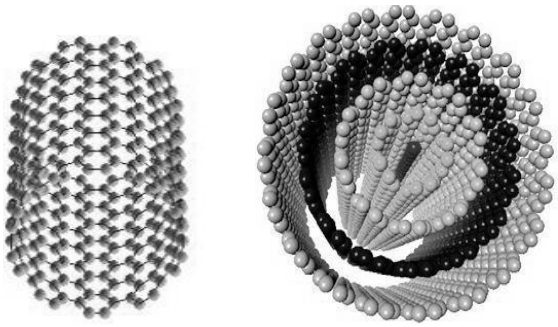


Fig.2. (a) Structure of SWCNT, (b) Structure of MWCNT

MWCNT consists of multiple concentric graphene cylinders, whose outer diameters may vary from a few to 100 nm. The spacing between the walls is 0.32 nm, which is the same as the spacing between graphene sheets in graphite [2]. The Structure of MWCNT is shown in Fig 2(b). In this paper, MWCNT is proposed as an alternate interconnect material for all three levels of interconnect. In order to validate the proposal, the performance analysis of MWCNT is carried out and compared with Cu and SWCNT interconnects using their equivalent circuit model.

This paper is organized as follows: Section II shows equivalent circuit models of Cu, SWCNT and MWCNT interconnect. Section III presents the results and compares the performance of copper, SWCNT and MWCNT interconnects. Section IV presents the conclusions.

II. EQUIVALENT CIRCUIT MODEL

A.COPPER INTERCONNECTS

The shrinkage in the feature size of Cu interconnects limits the interconnect performance and reliability in terms of delay, power and bandwidth. To analyze these parameters, equivalent RLC model is used as shown in Fig 3.

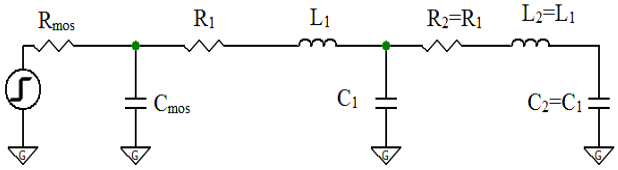


Fig. 3.Equivalent RLC model for copper interconnect

Using this model, interconnect resistance R, capacitance C and inductance L were calculated for various length.

$$R = \frac{\rho l}{wt} \quad (1)$$

$$C = \varepsilon\left[\frac{w}{h} + \left\{2.22\left(\frac{s}{s+0.7h}\right)^{3.19}\right\} + 1.17\left(\frac{s}{s+1.51h}\right)^{0.76}\left(\frac{t}{t+4.53h}\right)^{0.12}\right\}] \quad (2)$$

$$L = \mu l/2\pi[\ln(\frac{2l}{w+t} + \frac{1}{2} + \frac{0.22(w+t)}{l}] \quad (3)$$

$$M = \mu \frac{l}{2\pi\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right]} \quad (4)$$

$$\varepsilon = \varepsilon_r \times \varepsilon_o \quad (5)$$

Where R-Resistance, ρ-Resistivity, l-Length of interconnect, w-Width, s-Spacing, t-Thickness, d-distance between two layers, ε_o-Dielectric permittivity, ε_r-Relative dielectric permittivity of copper, μ -Permeability. In this paper, we have assumed that the spacing between interconnects s is equal to the interconnect width, i.e. $s = w$. Also the distance between two layers of interconnects d is assumed to be equal to twice as that of the interconnect width, i.e.d=2w. Furthermore, the thickness of the interconnect t ($t = AR \times w$) can be changed according to the aspect ratio (AR) [2].

B.CNT INTERCONNECTS

Carbon nanotubes (CNT) have emerged as a major research material in their application as very-large-scale integration (VLSI) interconnects for future IC's because of their excellent thermal conductivity, mechanical strength, large electron mean free paths, ballistic transport, and high current carrying capacity.

SWCNT INTERCONNECTS

As the feature size of Cu interconnects shrinks, which has performance degradation in interconnects. SWCNT has been proposed for the realization of future interconnects. SWCNT consists of a single sheet of graphene rolled up as hollow cylinder. The equivalent circuit model of SWCNT is shown in Fig 4. The equivalent circuit parameters are obtained using (6) – (10) [9].

$$R_f = \frac{h}{4e^2} \quad (6)$$

$$C_E = 2\pi \in \frac{1}{\ln\left(\frac{y}{d}\right)} \quad (7)$$

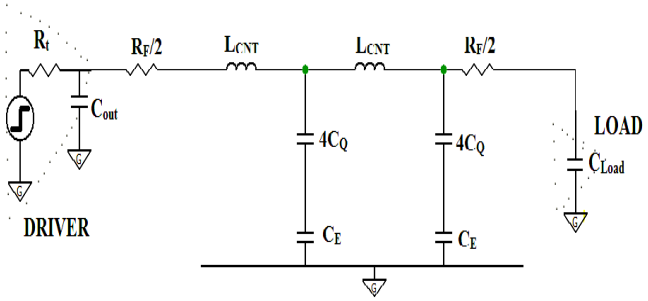


Fig. 4. Equivalent circuit model for SWCNT

$$C_Q = \frac{2e^2}{hv_f} \quad (8)$$

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right) \quad (9)$$

$$L_K = \frac{h}{2e^2 v_f} \quad (10)$$

Where R_f-Fundamental Resistance, C_E-Electrostatic capacitance, C_Q-Quantum capacitance, L_M-Magnetic inductance, L_K-Kinetic inductance, h-Planck's constant, ε-Electric field, y-Distance away from the ground, d-Diameter, e-Electron charge, v_f- Fermi velocity [9].

MWCNT INTERCONNECTS

MWCNT consists of several concentric graphene cylinders, whose outer diameter may vary from a few to 100nm, the spacing between the walls is 0.32 nm, the same as the spacing between graphene sheets in graphite. Each cylinder in MWCNT has different diameter. It has been confirmed both theoretically and experimentally that all shells within MWCNT can conduct if proper connections are made to all of them. High quality MWCNT has very large mean free path and operates in gigahertz frequency range. The theoretical models propose that long MWCNT with large-diameter can outperform Cu and even SWCNT interconnects. Hence it will be suitable for all level of interconnects. The number of channels can be calculated from the formula [3].

$$N = a.D + b, \quad D>3nm \quad (11)$$

Where constant a=0.0612 nm^{-1}, constant b=0.425,

D-diameter of the shell

$$D_i = D_{max} - 2r\,(i-1) \quad (12)$$

r- van der Waals gap, D_{max}- Outer shell diameter

The number of channels in i^{th} shell is given by

$$N = a.D_i + b \quad (13)$$

The equivalent circuit model of MWCNT is shown in Fig 5. The equivalent circuit parameters are obtained using (14) - (21) [3].

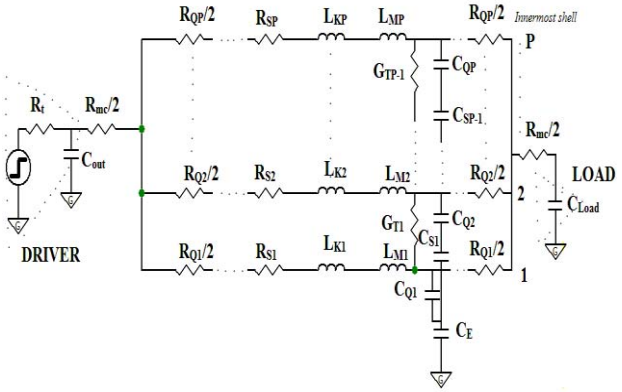


Fig. 5. Equivalent circuit model of MWCNT

$$R = R_Q + R_S.L = \frac{h}{2Ne^2} + \frac{h}{2Ne^2}\left(\frac{L}{\lambda}\right) \quad (14)$$

$$L_M = \left(\frac{\mu}{2\pi}\right)\cosh^{-1}\left(\frac{2H}{D}\right) \quad (15)$$

$$L_{K/Channel} = \left(\frac{h}{2v_f}\right)\left(\frac{1}{2}\right) = 8\ nH/\mu m \quad (16)$$

$$L_{K/Shell} = L_{\frac{K}{Channel}}/(a.D + b) \quad (17)$$

$$C_{Q/Channel} = 2\left(\frac{2e^2}{hv_f}\right) = 193\ aF/\mu m \quad (18)$$

$$C_{Q/Shell} = C_{Q/Channel} * (a.D + b) \quad (19)$$

$$C_S = \frac{2\pi\in}{\ln\left(\frac{D_{out}}{D_{in}}\right)} = \frac{2\pi\in}{\ln\left[\frac{D_{out}}{D_{out}-2d}\right]} \quad (20)$$

$$G_T = \sigma\pi D \quad (21)$$

Where R_Q-Quantum contact resistance, R_S-Scattering induced resistance, L-Length of the shell, λ-Mean free path (MFP), N-Number of conducting channels, L_M - Magnetic inductance, L_K - Kinetic inductance H-Separation between the nanotube center and ground, D-Diameter of each shell, C_Q-Quantum capacitance, C_S-Shell to shell capacitance, C_E-Electrostatic capacitance, G_T-Tunneling transconductance (negligible) .

III. PERFORMANCE COMPARISON OF COPPER AND CNT INTERCONNECTS

The evaluation circuit used for performance comparison of Cu, SWCNT and MWCNT is shown in Fig 6. In this circuit, the interconnect is implemented with Cu, SWCNT and MWCNT for various lengths using their equivalent circuits as shown in Fig 3, 4, 5 respectively. Resistance of Cu, SWCNT and MWCNT are compared for various lengths. This will provide a good insight to the performance analysis of MWCNT, Cu, and SWCNT at different levels of interconnect. It is observed that resistance of Cu is higher than SWCNT and MWCNT for longer lengths. Resistance of Cu, SWCNT and MWCNT are calculated from the equation (1), (6), (14) respectively. In this paper, all the three interconnects are simulated in HSPICE and their results are compared in terms of delay, resistance and capacitance for all the three levels of interconnect. MWCNT has less signal attenuation than Cu and SWCNT as shown in Fig 7. The simulation results of Cu, SWCNT and MWCNT at all the three interconnect level is shown in Fig. 7(a), 7(b), 7(c).

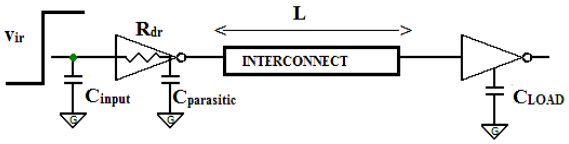


Fig. 6. Performance evaluation circuit.

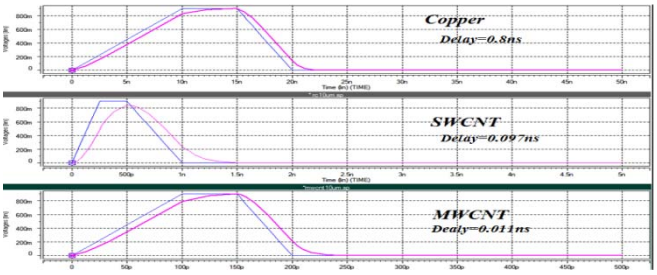


Fig. 7(a). Simulation result of Cu, SWCNT, MWCNT at local interconnect level.

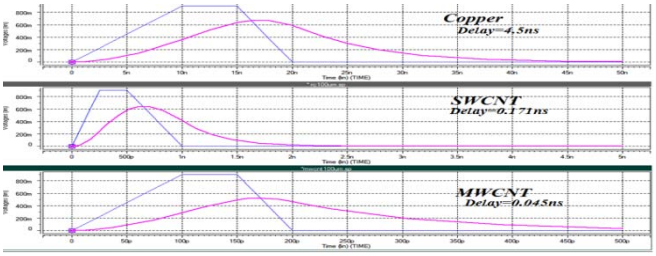


Fig. 7(b). Simulation result of Cu, SWCNT, MWCNT at intermediate interconnect level.

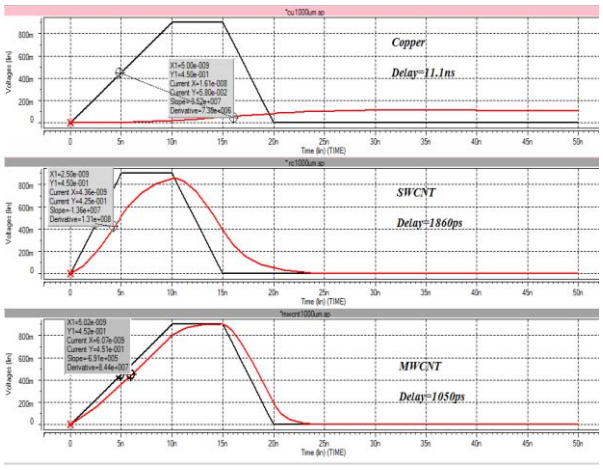


Fig. 7(c). Simulation result of Cu, SWCNT, MWCNT at global interconnect level.

From the above simulation results, the measurement of delay for all the three interconnects at different level is shown in table 1.

Table.1. Delay comparison of Cu, SWCNT, MWCNT interconnect

Interconnect level	Copper	SWCNT	MWCNT
Local	0.8ns	0.097ns	0.011ns
Intermediate	4.5ns	0.171ns	0.045ns
Global	11.1ns	1.86ns	1.05ns

LOCAL INTERCONNECT

The local interconnects are the shortest interconnects used to connect adjacent gates or devices. The length of the interconnect is in the range of few hundred nanometers to few micrometers. It has high resistance because of the small area of cross section. MWCNT has better performance than copper because it uses CNT with smaller diameter and hence it achieves ballistic transport.

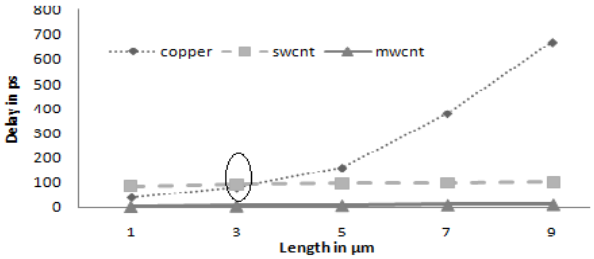


Fig. 8. Delay comparison at local interconnect

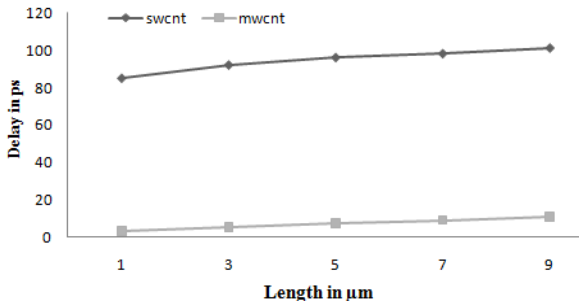


Fig. 8. (a) Delay comparison of SWCNT and MWCNT at local interconnect

Fig 8 shows the comparison of Cu and CNT. It is observed that MWCNT has better delay performance because of its low resistance. While comparing the SWCNT and MWCNT, the SWCNT has higher delay than MWCNT as shown in Fig 8(a). The capacitance of CNT is higher than that of the Cu wires across all technology generations. The delay of Cu is less than SWCNT below 3µm above which SWCNT has lower delay than Cu at the local interconnect level, this is indicated in Fig 8. MWCNT has better delay than both Cu and SWCNT, which is about 60% less than that of Cu and 10% less than SWCNT. This is because MWCNT has less delay than Cu.

INTERMEDIATE INTERCONNECT

The intermediate interconnects are also called semiglobal interconnects and used to make connection between the logic blocks inside the IC. Its length ranges from tens of micrometer to five hundred micrometer. Fig 9 shows the comparison of Cu and CNT at the intermediate level. Both SWCNT and MWCNT have better delay performance over Cu. MWCNT shows increasingly better delay performance over SWCNT with increasing interconnect length. MWCNT is 100 times better than Cu and four times better than SWCNT in terms of delay. Fig 9(a) shows delay comparison of SWCNT and MWCNT

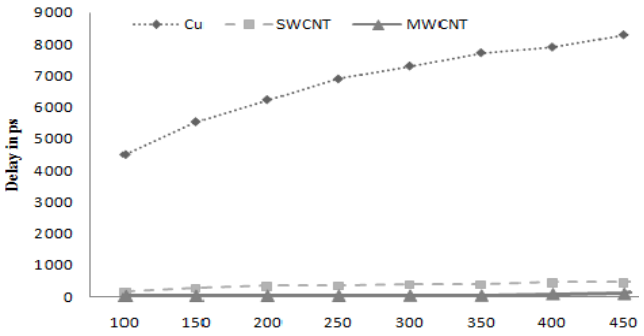


Fig. 9. Delay comparison at intermediate interconnect

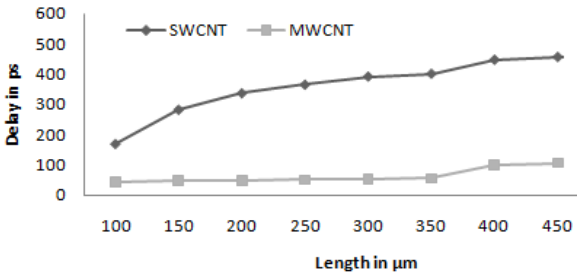


Fig. 9. (a) Delay comparison of SWCNT and MWCNT at intermediate interconnect

GLOBAL INTERCONNECT

Global interconnects are the longest interconnects that run across the chip. It ranges in the order of millimeters. It has larger cross sectional area. The delay comparison between MWCNT, SWCNT and Cu interconnect at the global level is shown in Fig 10. It shows that CNT has lower delay than Cu. Delay comparison of SWCNT and MWCNT at global interconnect is shown in Fig 10(a). MWCNT have less delay, higher bandwidth than SWCNT. Delay comparison of all interconnects are shown in Fig 11.

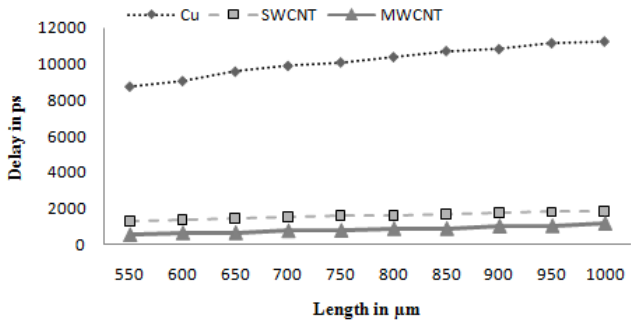


Fig. 10. Delay comparison at global interconnect

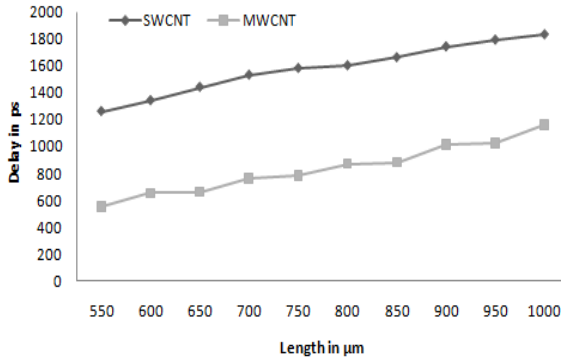


Fig.10. (a) Delay comparison of SWCNT and MWCNT at global interconnect

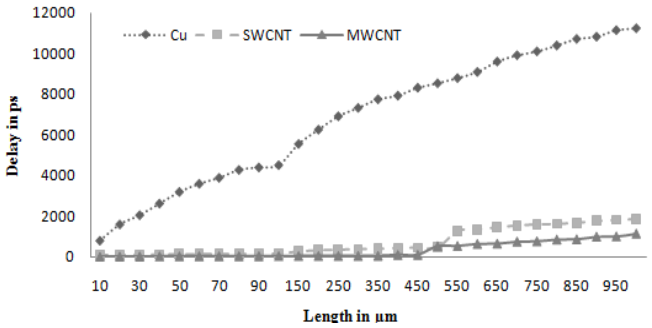


Fig. 11. Delay comparison in all interconnects

IV.CONCLUSION

In this paper, we have compared the performance of CNT (SWCNT and MWCNT) on- chip interconnect with that of Cu interconnects. Simulation results show that MWCNT has much low delay compared to SWCNT and Cu in local, semiglobal and global interconnects. It is clearly shown that MWCNT is 100 times better than Cu and four times better than SWCNT in terms of delay. This shows that MWCNT has significant prospect for future VLSI-interconnect applications. Hence, MWCNT may be used in place of copper to achieve higher performance in future ICs.

REFERENCES

[1] Ahmet Ceyhan, and Azad Naeemi, "Cu Interconnect Limitations And Opportunities For SWCNT Interconnects At The End Of The Roadmap "-IEEE Transactions On Electron Devices, Vol. 60, No. 1, January 2013.

[2] Harpreet Singh Bhatia, Mayank K. Rai "A Comparative Study Of Delay Analysis for Carbon Nanotube And Copper Based VLSI Interconnect Models"-July 2011.

[3] Hong Li, Wen-Yan Yin, Kaustav Banerjee, and Jun-Fa Mao "Circuit Modeling And Performance Analysis Of Multi-Walled Carbon Nanotube Interconnects"- IEEE Transactions On Electron Devices, Vol. 55, NO. 6, June 2008 .

[4] "International Technology Roadmap For Semiconductors 2009 Edition Interconnect".

[5] "International Technology Roadmap For Semiconductors 2007 Edition Emerging Research Materials" .

[6] Jeff Gambino, Fen Chen, John He Ibm Microelectronics "Copper Interconnect Technology For The 32 Nm Node And Beyond" 2009.

[7] Kyung-Hoae Koo "Comparison Study Of Future On-Chip Interconnects For High Performance VLSI Applications"- March 2011.

[8] Kyung-Hoae Koo, Hoyeol Cho, Pawan Kapur, And Krishna C. Saraswat "Performance Comparisons Between Carbon Nanotubes, Optical, And Cu For Future High-Performance On-Chip Interconnect Applications"- IEEE Transactions On Electron Devices, Vol. 54, No. 12, December 2007.

[9] Navin Srivastava And Kaustav Banerjee "Performance Analysis Of Carbon Nanotube Interconnects For VLSI Applications"2005.

[10] Saraswat "Interconnect Scaling".

[11] Penny Beebe, Amit Lal, Alan Yu "A Study of Carbon Nanotubes and their Applications in Transistors"2004.

[12] M. Haselman, S. Hauck, The future of integrated circuits: a survey of nanoelectronics, Proc. IEEE 98, no. 1 pp. 11-38, 2010. doi:10.1109/JPROC.2009.2032356.

[13] 7. A. Maffucci, Carbon nanotubes in nanopackaging applications, *IEEE Nanotechnol. Mag.* 3, no. 3 pp. 22-25, 2009. doi:10.1109/MNANO.2009.934214.

[14] 8. A. G. Chiariello, G. Miano, A. Maffucci, Carbon nanotube bundles as nanoscale chip to package interconnects, *Proc. 9th IEEE Conf. Nanotechnol.,* pp. 58-61, 2009.

[15] 9. J.-H. Ting, C.-C. Chiu, F.-Y. Huang, Carbon nanotube array vias for interconnect applications, *J. Vac. Sci. Technol. B* 27, no. 3pp. 1086-1092, 2009. doi:10.1116/1.3123330.

[16] 10. N. Alam, A. K. Kureshi, M. Hasan, T. Arslan, Carbon nanotube interconnects for low-power high-speed applications, *Proc. IEEE Int'l Symp. Circ. Syst.,* pp. 2273-2276, 2009. doi:10.1109/ISCAS.2009.5118252.

[17] 11. M. R. Stan, D. Unluer, A. Ghosh, F. Tseng, Graphene devices, interconnect and circuits, Proc. IEEE Int'l Symp. Circ. Syst., pp. 69-72, 2009. doi:10.1109/ISCAS.2009.5117687.

[18] 12. N. Srivastava, L. Hong, F. Kreupl, K. Banerjee, On the applicability of single-walled carbon nanotubes as VLSI interconnects, *IEEE Trans. Nanotechnol.* 8, no. 4 pp. 542-559, 2009. doi:10.1109/TNANO.2009.2013945

[19] 13. H. Li, C. Xu, N. Srivastava, K. Banerjee, Carbon nanomaterials for next-generation interconnects and passives: physics, status, and prospects,*IEEE Trans. Electron Dev.* 56, no. 9 pp. 1799-1821, 2009. doi:10.1109/TED.2009.2026524.

[20] Ashok Srivastava, Yao Xu and Ashwani Sharma" Carbon nanotubes for next-generation interconnects"2010.

[21] Bakoglu, H. B. Circuits, Interconnections and Packaging for VLSI. Addison-Wesley Publishing Company, Reading, Massachusetts, 1990.

[22] Neemi, et al, "On-chip interconnect network at the end of roadmap limits and nanotechnology approach" 2006.

[23] "International Technology Roadmap For Semiconductors 2011 Edition Interconnect.