High Efficiency Biquad Infinite Impulse Response Filter using Charge Recovery Logic Family

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ABSTRACT- Charge recovering circuit has the potential to reduce dynamic power consumption in digital systems with significant switching activity. A charge recovery logic family named Enhanced Boost Logic has been presented. EBL is an enhanced version of Boost Logic that achieves shorter pipeline latencies while retaining its energy advantages over static CMOS. The paper present Biquad IIR filter. The design yields lower latency while maintaining good energy efficiency. The EBL based Biquad IIR filter is designed. EBL achieves High speed and low power operation. The EBL energy advantage over static CMOS Design.

Index terms; Digital Signal Processing (DSP), low power VLSI, Infinite Impulse Response(IIR).

I. INTRODUCTION

Demands for low power electronics have motivated designers to explore new approaches to VLSI circuits. The classical approaches of reducing energy dissipation in conventional CMOS circuits included reducing the supply voltages ,node capacitance, and Switching frequencies Energy-recovery circuitry, on the other hand, is a new promising approach to the design of VLSI circuits with very low energy dissipation.

Charge-recovery circuitry has potential reduce dynamic power consumption in digital systems with Significant switching activity. To keep energy consumption to a minimum, charge-recovery circuitry is typically designed so
that it maintains low voltage drops across device channels, while recovering the charge supplied to it every clock cycle[1].

It introduces the Enhanced Boost Logic (EBL), an improved version of the basic Boost Logic that achieves shorter pipeline latencies while retaining its energy advantages over static CMOS. Similar to Boost Logic, EBL is capable of operation at high clock frequencies by developing a near-

threshold voltage before the onset of the power clock. Evaluation devices in EBL have twice the gate overdrive compared to first-generation Boost Logic [2], [3].

The biquad has a necessary coefficient scaling factor when one or more of the coefficients are greater than 1.0. This filter has a 16-bit input, 16-bit output and 16-bit coefficients. This code lets the ADSP-2100 Family DSP perform a Nth-order IIR filter by performing N/2 biquads. The execution time is [8*(N/2) + 10] instruction cycles. The DSP can perform a tenth-order IIR filter on a signal sampled at more than 300 k Sa/s.

The latency of this EBL-based IIR is only 1.5 cycles longer than that of a similar-performance static CMOS design that has been implemented separately. Fabricated in a 0.13- m CMOS process, the test-chip includes a fully-integrated 3 nH inductor.

II ENHANCED BOOST LOGIC

Powered by the aggressively-scaled voltage, the Logic stage drives the dual-rail outputs conventionally with sub threshold-level energy consumption the first half of each clock cycle. Subsequently, during the second half of each cycle, the Boost stage amplifies the near-threshold voltage between the two outputs to full rail using the two complementary clock phases pc and pc_ b. These clock phases are generated using an H-bridge topology. The energy-efficient and multi-MHz operation of SBL with a single sub threshold supply has been demonstrated in silicon [4], [5].

Each EBL gate has two stages: Evaluation and Boost. Similar to SBL, the Boost stage consists of a cross-coupled inverter with the source of the pMOS connected to a charge recovering clock phase , enabling high performance through enhanced gate overdrive. Unlike SBL, however, the Evaluation stage relies on an nMOS precharge device for pull-up, instead of a complementary pull-up network, thus increasing performance by avoiding the series-connected devices in the pull-down network (PDN). The bulk of all nMOS

Transistors are connected to ground, and the bulk of pMOS transistors in the cross-coupled inverters are connected to the corresponding power-clock phases.

Another departure from Boost Logic is that the same sub threshold supply is used to power a “blip” clock generator, producing two partially-overlapping clock waveforms and with peak values significantly greater than VCC. The bulk of all NMOS transistors are connected to ground, and the bulk of PMOS transistors in the cross-coupled inverters are connected to the corresponding power-clock phases.

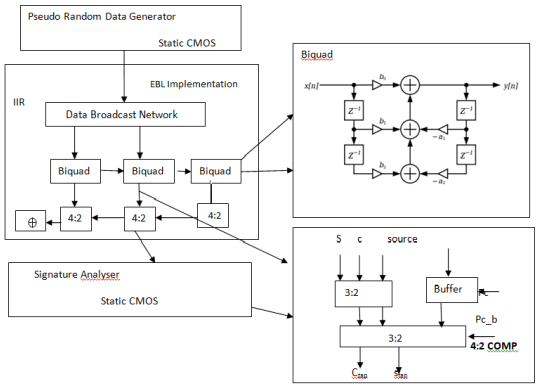


Fig 1 IIR block diagram and clock generator

EBL improves upon Boost Logic in three ways. First, the use of a single near-threshold DC supply in the Evaluation stage reduces the number of power supplies required and doubles the gate overdrive. Second, the PDN of EBL gates enables the implementation of more complex functions. Specifically, by relying on a blip clock generator with two almost-non-overlapping phases, EBL eliminates the need for a clock-gated device in its PDN.

The 2 gate overdrive allows more complex functions to develop the near-threshold difference between the dual-rail outputs by the end of the Evaluation phase. Therefore, the maximum pull-down stack height of an EBL gate can be higher than in Boost Logic.

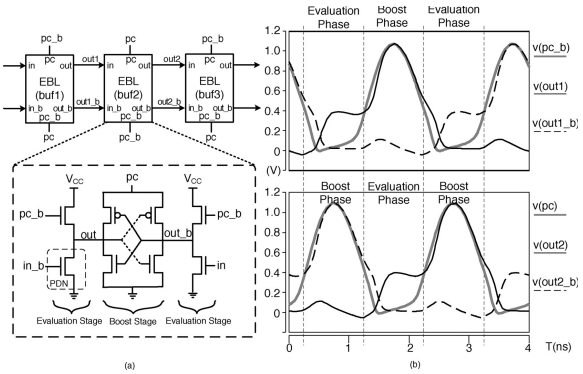


Fig 2 EBL Buffer schematic diagram

Per-cycle energy consumption of an EBL gate is given by the equation

$$E_{\mathrm{EBL}} = E_{\mathrm{Evaluation}} + E_{\mathrm{Boost}} + E_{\mathrm{Crowbar}}$$

III. TEST-CHIP OVERVIEW

EBL gate has a built-in transparent latch, the state intensive nature of a transpose-type FIR filter coupled with the relatively simple combinational logic between its state elements. The FIR filter is pipelined to take advantage of EBL's potential for low latency overhead. Input data are broadcast to each tap within 1 cycle. Each 8x 8 multiplier takes 1.5 cycles to merge the partial products from the Booth mux to the sum and carry.

Table 1

Cell name	Power dissipation	Average delay	Worst case delay	Average PDP	Worst case PDP	Operation frequency
FA_con	100%	100%	100%	100%	100%	100%
FA_new	67%	104%	124%	70%	84%	87%
FA_sD	74%	79%	95%	58%	71%	113%

Table 1 Comparison Of Different Full Adders

The IIR filter is pipelined to take advantage of EBL's potential for low latency overhead. Input data are broadcast to each tap within 1 cycle. Each tap takes 1 cycle to merge the sum and carry vector pairs from the previous tap and the 8x 8 multiplier. The vector pairs are then merged in a 20-bit hybrid carry-look-ahead/carry-select adder with two cycles of latency.

The longest path through the EBL-based FIR has a latency of 18.5 cycles. Compared to other high-performance low-latency arithmetic implementations, the latency overhead of the EBL-

based IIR is 1.5 cycles: 0.5 cycle in the 8x 8 multiplier, and 1 cycle in the 20-bit adder.

The 4:2 compressor array is formed by a series of 4:2 compressors cascaded together it together, is used to perform column-wise compression of the partial produce.The Sum function has an evaluation stack height of six, and the Carry function has an evaluation stack height of five.

The 121.6 m layout implementation of the 4-to-2 compressor in EBL, which has only 7.6% area EBL to static CMOS, a sense-amplifier flip-flop converts signals from an EBL gate output to a standard digital signal. The BIST circuits around the FIR filter, such as the pseudo-random sequence generator, the signature analyzer, and the signature generator, are implemented using standard cells.

The output of the pseudo-random sequence generator is sent to convert buffers, and the outputs of the FIR are digitized by the sense-amplifier flip-flops before being processed by the signature analyzer.

TABLE 2

Design type	Biquad	14 tap 8 bit	8tap 6 bit	14 tap 8 bit
Technology	0.13µm	0.13µm	0.18µm	0.13µm
Normal supply	1.0	1.2	1.8	1.2
Operating frequency	450	466	225	1010
Sample rate(M/samples)	450	466	550	1010
Power dissipation(mW)	40.0	39.1	36	122.5
Area(mm2)	0.3	0.34	0.3	0.85
Power/MHz/Tap/In bits/Coeff bits	90.6nW	93.6nW	230nW	133nW

Table 2 Comparison Of Different Filters

IV. EBL DESIGN METHODOLOGY

Charge-Recovery logic has been designed using transistor- level simulation to verify functionality and electrical properties. The number of simulation cycles it takes to excite all possible input combinations and all possible timing arcs is at least exponential with the number of inputs. Even with the use of fast Spice programs such as Synopsys HSIM or Cadence.

This methodology enables the use of switch-level Verilog simulation. More importantly, it enables the use of industrial static timing analysis tools to verify the electrical properties of an EBL design. It describes the approach to switch-level netlist generation for Verilog simulation and LVS check using the same schematic.

It describes process to generate a LIBERTY format model file (.LIB) for the static timing analysis tools to verify electrical properties to switch- level Verilog netlist generation, the Evaluation stage is converted to complementary combinational logic. The pull-up precharge devices in the Evaluation stage.

The use of these weak devices eliminates the possibility of having contention between the precharge devices and the pull-down networks in Verilog simulation. The Boost stage is netlisted as a pair of transparent latches, one for the true output and another for its complement. To netlist the Boost stage

as a pair of transparent latches, the input and the output of the Boost stage need to be separated.

A larger voltage difference across the outputs at the onset of the power clock implies that the Boost stage would be able to amplify the differential output pair more efficiently, in which case the outputs would track the power-clock more closely since this requirement yields a delay between the power clock and the output during the Boost phase to be less than 10% of the cycle time, yielding a smaller voltage drop across the cross-coupled pMOS devices in the Boost stage.

V SIMULATION RESULTS

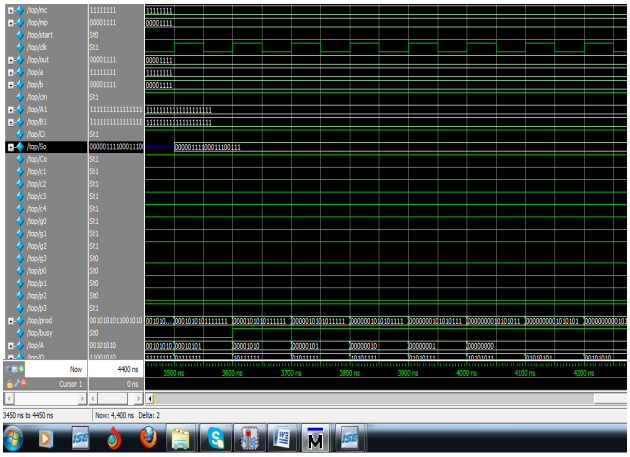


Fig 3 screenshot for output module

output analysis If the start signal is 1

A<=8'b0

M<=mc

Q<=mp

Q-1<=1'b0

Count<=4'b0

Default count<=count+1'b1

The energy requirements of the voltage-scaled conventional FIR and the EBL-based FIR in self-resonant mode for a range of operating frequencies. For clock frequencies above 350 MHz, the EBL FIR filter exhibits 21–34% energy savings over its conventional counterpart. Below 350 MHz, the large inductors required to oscillate the

system have poor quality factor due to their large dimensions and high turn counts, increasing the energy requirements of the EBL design compared to its conventional counterpart.

VI CONCLUSION

The proposed results is to designed EBL based Biquad IIR filter. The Butterworth filter is to achieves low power and high speed operation. The Biquad filter achieves lower latency delay and good energy efficiency. At its resonant frequency of 450 MHz, the test-chip dissipates 40.1 mW with a 90.6 nW /MHz/Tap/InBit/CoeffBit

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