Journal of Intelligent & Fuzzy Systems 42 (2022) 5939–5956
DOI:10.3233/JIFS-212583
IOS Press

Design and experimental investigation on VL-MLI intended for half height (H-H) method to improve power quality using modified particle swarm optimization (MPSO) algorithm

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Abstract. A Voltage lift performance is an excellent role to DC/DC conversion topology. The Voltage Lift Multilevel Inverter (VL-MLI) topology is suggested with minimal number of components compared to the conventional multilevel inverter (MLI). In this method, the Modified Particle Swarm Optimization (MPSO) conveys a primary task for the VL-MLI using Half Height (H-H) method, it determine the required optimum switching angles to eliminate desired value of harmonics. The simulation circuit for fifteen level output uses single switch voltage-lift inverter fed with resistive and inductive loads (R & L load). The power quality is developed by voltage-lift multilevel inverter with minimized harmonics under the various Modulation Index (MI) while varied from 0.1 up to 1. The circuit is designed in a Field Programmable Gate Array (FPGA), which includes the MPSO rules for fast convergence to reduce the lower order harmonics and finds the best optimum switching angle values. To report this problem the H-H has implemented with MPSO to reduce minimum Total Harmonic Distortion (THD) for simulation circuit using Proteus 7.7 simulink tool. Due to the absence of multiple switches, filter and inductor element exposes for novelty of the proposed system. The comparative analysis has been carried-out with existing optimization and modulation methods.

Keywords: Solar-Photovoltaic, voltage lift-multilevel inverter, particle swarm optimization algorithm, half height, field program gate array

1. Introduction

The electrical system has major problems due to the presence of harmonic contents in the power quality features. The harmonics may be classified into

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two types: voltage harmonics and current harmonics [1]. Voltage harmonics and current harmonics cause in an electric power system are a result of non-linear electric loads. The harmonics in electrical system results are increased heating equipment in resistive load, pulsating torque in induction motor drives, and the conductors to make power losses, high Electro Magnetic Interferences (EMI) problem. Thus the Reduction of THD is considered to enhance efficiency and improve the energy quality in most industrial and consumer applications. The current harmonics usually occurs by non-linear loads. Whenever a non-linear load such as rectifier (or) inverter is attached to the system, it draws a current that's not necessarily sinusoidal. The harmonics are produced by neither source of the foundation nor the load side. The usage of non-linear loads such as converters, computer devices, printers and etc., the multilevel inverters are introduced in power conversion system. Ultimately it is recognized as a device that plays major roles in power electronics. In general, the multi-level inverter is categorized into three types: Conventional Multi-Level Inverter (CMLI) [2], Modular Multi-Level Inverter (MMLI) [3], generalized multilevel cells [4], and also some emerging multilevel inverter [5] topologies such as mixed-level hybrid Multilevel cells [6], soft switched multilevel inverter [7]. Particularly, it will be helpful for multilevel output voltage with increasing levels.

The absence of fossil fuels and the greenhouse effect, the need for sustainable energy has increased dramatically over time. The solar photovoltaic has the advantage of direct conversion of sunlight to electricity and also well suitable for most of the regions, therefore it is highly preferred when compared to other renewable energy sources [8, 9]. Pulse width modulation (PWM) and multilevel modulation (MLM) are the two forms of DC/AC conversion techniques. Various inverter topologies are offered for DC/AC conversion in solar PV systems, with the multilayer inverting technique horizontally collecting levels to attain the waveform [10, 11]. Many levels are generated from numerous clamping diode, clamping capacitor, and DC sources, which is a disadvantage of this converter design. The requirements of Power Quality (P-Q) depends on the voltage or current for either input or output side within certain boundaries. The P-Q is still a major universal issue that outcome is enriched by power converters. The electrical power is enhanced by energy resources that have rapidly simulated the change of energy resources every year which has been estimated by Spence dale BP statistical review of world energy June 2020 (69th edition). In renewable power which continued to grow up rapidly in the preceding year, i.e., solar power installation represents at 585 GW a net increase of 98 GW, and that is 20% points higher than 2019. The electrical power is delivered to the load or temperature variation in electrical apparatus such as resistor, inductor, and motor drives. That includes excessive sudden changes like voltage/current unbalance, voltage drop, and harmonic distortion. Power factor plays a key role in improving the efficiency of the electrical systems as projected by [12]. The P-Q issues are formed in Non-Linear Load (N-LL) or distribution side, due to some energy losses and poor Reactive Power Compensation (RPC). These are the problems that appeared nowadays in all Electrical Load (EL) [13]. As a result, the general usage of EL such as resistance, inductance loads is attained major problems in harmonic content and change of impedance values across the load. If reducing the discharging negative sequence of voltage or current supply across the load terminals are enhanced to improve P-Q with the help of DC-link capacitors [14].

The alternating electrical unit charges are generated in the form of a sinusoidal waveform. It can be measured the parameters such as voltage, current, power factor, and efficiency. At any time, the current is proportional to the voltage is known as linear load. The linear load power factor is always near to one, i.e., incandescent light, heaters-Resistive (R) load [15]. The nature of non-linear load generates lower or higher-order harmonics in the current waveform. Due to the distortion of the current leads in to the distortion of voltage. Under these conditions, the voltage waveform is no longer proportional to the current, i.e., change of impedance value and temperature across the loads like Alternating Current (AC) motor, Resistive-Inductive (RL) load (heater, laser printer, electronic ballast, and refrigerator). The quality power in RE systems is a very significant feature in the recent scenario for all non-linear load connected system, due to unbalanced real and reactive power disruption in electric power networks [16].

Therefore, these loads generate disturbances in the output waveform, particularly in N-LL. It has changed into an effectively predicted part of the interest in recent years because of the electrical load affects. The consumer electrical appliances draw the supply in electrical networks. The electric supply

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flow through the semiconductor switches, which control the output (load) system. But, the recent scenario increase fluctuation, and harmonics appear in a load of distribution. It leads to the consequences of consumer appliances [17]. Hence to solve these issues should be minimized electrical components such as semiconductor devices, transformer, DC sources, and DC link capacitors, etc. Renewable and sustainable energy is growing up day by day, and the need for power demand is also increasing regularly. Nowadays in all countries, due to constantly increment in the quantity of environmental pollution and greenhouse gases, the availability of RE power is generated in many countries by more emphasis on using power resources such as solar, wind, and hydroelectric. The energy storage devices are estimated to achieve maximum energy from S-PV panels in the day time, and the batteries are the most widely used off-grid RE storage devices all over the world [18]. Therefore, the need for reactive power enhancement by using energy storage devices, and it has been furthermore more energy developed by power converters with implementing some optimization control strategy.

There are many advantages are in S-PV model, (1) Grid connected system such as micro-grid or mini-grid is possible to associate with S-PV power plant, (2) S-PV panel is fed with linear or non-linear motor load conditions interface with power inverters, (3) low consumption charges compared to the other RE and pollution-free, and (4) DC power is generated frequently in a peak S-PV irradiation conditions. A feature development of the metaheuristics algorithm, it has been the establishment of a nature-inspired approach based on the three categories [19], (1) Single metaheuristics solution, (2) Based on the population, and (3) Hybrid metaheuristics. The swarm and memory based emerging intelligent optimizations are performed based on intermediate, direction, and population approaches. Due to the nature-inspired algorithm, the current velocity point is to move into a new velocity search point.

To minimize the objective function to lower value. Therefore, there are no issues to associate with both FA and PSO, the optimization problem and solution should be formulated by using the design of fundamental variables, which are mainly utilized throughout the optimization process. The next stage is optimization problem solving, it has been used to associate with constraints obtained and it represents in the design of variable parameters that must be identified. Due to some certain phenomena and resource limitations are included in the objective function. Based on the algorithm principle, there are two possibilities in the objective functions, minimization (or) maximization. A 15-level inverter, it is established a population of candidate solutions to give a new search point and accelerate the switching angle values are within the minimum computational time in integrated PV proposed scheme [20]. PSO implementation of calculating switching angle (θ_1, θ_2, $\theta_3 \ldots .$, θ_n) and gate signal values for the relevant inverter power devices, which are proposed with equal DC source, and determine the lower order harmonics of the inverter [21]. The bio-inspired algorithm applied in PWM inverter, it has been applied for renewable power conversion and application [22–25]. It's included the swarm-based intelligent analysis in terms of performance computational parameter, convergence speed, and accuracy. The speed of the computational and convergence of the swarms are obtained THD level gives a very high essential performance with finding the best optimum solution associate with the other methods such as modified genetic optimization algorithms. These drawback of this converter topology includes have increase number of repeating parts and synthesized from several DC voltage sources required. In this investigation depends on least number of components and minimize the number of levels. The proposed VL-MLI increases the output voltage gain with the control of the modulation index, and decreases the voltage drop across the load with the help of series capacitor unit (C_2-C_8), it is comparable to traditional and multilevel modular inverters. The voltage-lift inverter is suitable for reactive power compensation and for providing the desired alternating output waveform. Therefore, design and development of modified VL-MLI fed into linear and non-linear load conditions as shown in Fig. 1. The H-H approach can be compute with MPSO, it uses to make the best optimal switching angles and to find out the low order harmonics value. The input sources from solar-PV are series connected MLI which works and lifts up a voltage which is encouraged into different load conditions (R & L load). The solar VL-MLI differ from classical inverters, as individual voltage-lift inverters is attached to one are more number of solar panel (S_{PV1}-S_{PV4}). This can improve the overall efficiency of the system. It has been furthermore development using ISIS Proteus 7.7 simulink software and FPGA prototype model with better power quality improvement and it is used in medium and low power applications, particularly in renewable power electronics utility.

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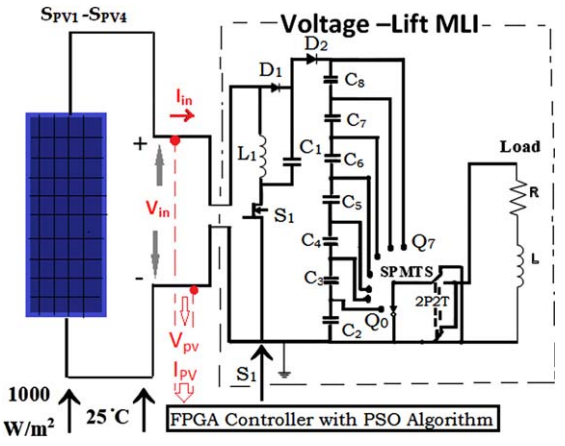


Fig. 1. Proposed Voltage-lift multilevel inverter.

2. PV Source and modulation scheme

Solar photovoltaic (PV) panels are a versatile energy technology that can help electrical customers of all kinds with their electricity needs. There are two main categories of solar panel installation: 1. Grid connected PV, 2. Standalone PV. They are primarily differ in size and location, and also are unique in several other system characteristics. PV installations may be residential, commercial or industrial, utility-scale, ground-mounted, rooftop mounted, and wall mounted or floating etc., [26]. The need of several sources on the DC side of the converter makes attractive multilevel technology for photovoltaic applications. In this regards, a solar voltage-lift multilevel inverter is a standalone off-grid Balance of System (BOS) component of a photovoltaic module [27] and it can be used in off grid systems like Electric vehicles and R, & L load connected system [28]. The BOS encompasses all components of a photovoltaic system other than the photovoltaic panels. This includes wiring, switches, a mounting system, a battery bank, battery charger and one or many solar multilevel inverters etc... This type of solar voltage-lift multilevel inverters have special functions adapted for use with photovoltaic arrays, includes maximum power point (MPP) tracking.

The solar-PV four modules is normally designed as series connected modules per string 9, number of cells per module 96, and number of parallel per string 250 as shown in Fig. 2. There are four PV module parameters photo-generated current (Iph), diode saturation current (Isat), parallel resistance (Rp), and series resistance (Rs) adjusted to fit the following four module characteristics measured under standard-test condition (STC: Irradiance-1000 W/m2, Diode Quality factor (Qd), and cell temperature-25°C) as in shown in as shown in Table 1. The PV arrays consist of Number of parallel (Npar) PV strings of modules are connected in parallel, each string consisting of Number of series (Nser) PV string connected in series.

The Solar-PV made by supply are open circuit voltage (V_{oc})-64.2 V, short circuit current (I_{sc})-5.96A, voltage at maximum power point (Vmp)-54.7, current at maximum power point (Imp)-5.58. In the photovoltaic arrays (SPV_1-SPV_4) the terminal voltage is not equal to the maximum power point (MPP), when the PV-module output voltage is verified in day time. The quantity of modules wired in series multiplied by the Vmax equals to maximum system voltage 4*16.07 = 64.28 V maximum system power input (P_{in}) voltage and current 5.96A as shown in Fig. 3. This can improve the overall efficiency of the system. The basic expression for maximum efficiency (η) of a photovoltaic cell is given by the ratio of output power to the incident solar power.

$$\text{Fill Factor (F.F)} = \frac{P_{in}}{V_{oc} \times I_{sc}} \tag{1}$$

$$\eta = \frac{V_{oc} I_{sc} FF}{P_{in}} \tag{2}$$

When the panel output voltage is lowered due to cloudy condition during checking of PV-module in day time, the MPP (P&O) controller is adjusts the voltage by a small amount from the array open circuit voltage and short-circuits current improved by Perturb and Observe rule. Solar tracker integration and improved P&O MPPT algorithm were provided better quality and controlled electricity to the load. The voltage of the module is regularly compared with the corresponding output power in the previous approach. The input sources from solar-PV are connected with the voltage lift DC-AC converter which works and lifts up a voltage which is encouraged into linear and non-linear load (R & RL load).

3. Voltage lift multilevel inverter approach

The VL-MLI is basically consists of only one MOSFET Switch, seven series switching capacitor, and two Freewheeling diodes to generates fifteen level output (+Q_7 0 & - Q_7), (+Q_6 0 & -Q_6), (+Q_5 0 & -Q_5), (+Q_4 0 & -Q_4), (+Q_3 0 & -Q_3), (+Q_2 0 & -Q_2), and (+Q_1 0 & - Q_1) in Fig. 4. Whereas con-

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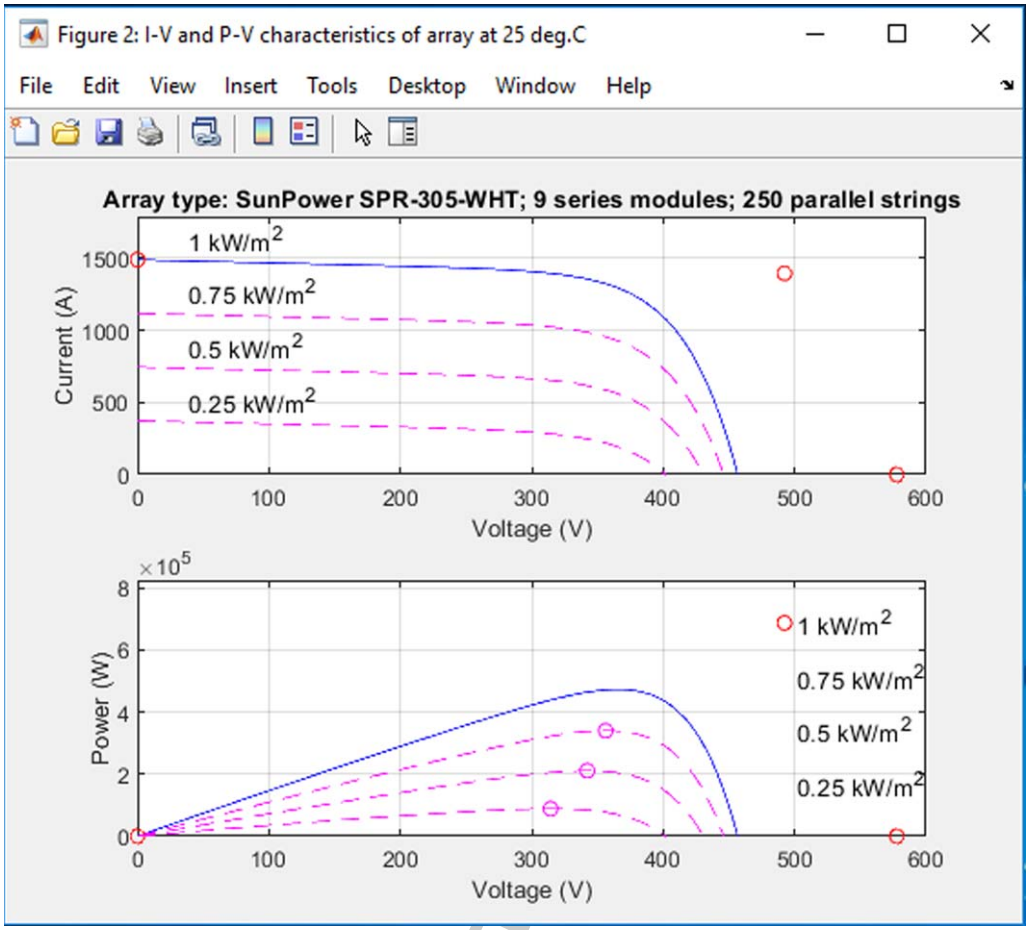


Fig. 2. Solar-irradiation conditions.

Table 1
Deviation report of PV- module with/without MPPT

Description	Without MPPT using proposed MLI	With MPPT using proposed MLI
Maximum power (Pmax)	55–60 watts	65 watts
Voltage at Pmax (Vmp)	51 V	54.7 V
Current at Pmax (Imp)	4.95 A	5.58 A
Open-circuit voltage (Voc)	59.5 V	64.2 V
Short-circuit current (Isc)	4.51 A	5.96 A

ventional, Modular, and Generalized MLI requires twelve switches to generate the fifteen level of output as shown in Table 2. The number of node voltages are Q_7 up to Q_1. The purpose of the capacitor voltage (E_m) for each capacitor is to function as the capacitor bank unit.

$$Em = \frac{V_{dc}}{N-1} \tag{3}$$

Where N denotes number of levels.

The capacitor band switch (or) single pole multi-through switch (SPMTS) Turn on positive output terminal voltage from Q_7, Q_6, Q_5, Q_4, Q_3, Q_2, Q_1, & Q_0 and negative output terminal voltage turn off are $-Q_7$, $-Q_6$ $-Q_5$,$-Q_4$,$-Q_3$,$-Q_2$, & $-Q_1$ respectively in VLMLI. The operation of VL-MLI, when the main switch S is ON, the capacitor and (C_1) inductor (L_1) are charged by the Source voltage (V_{DC}) during switching on period (kT). In the steady state condition

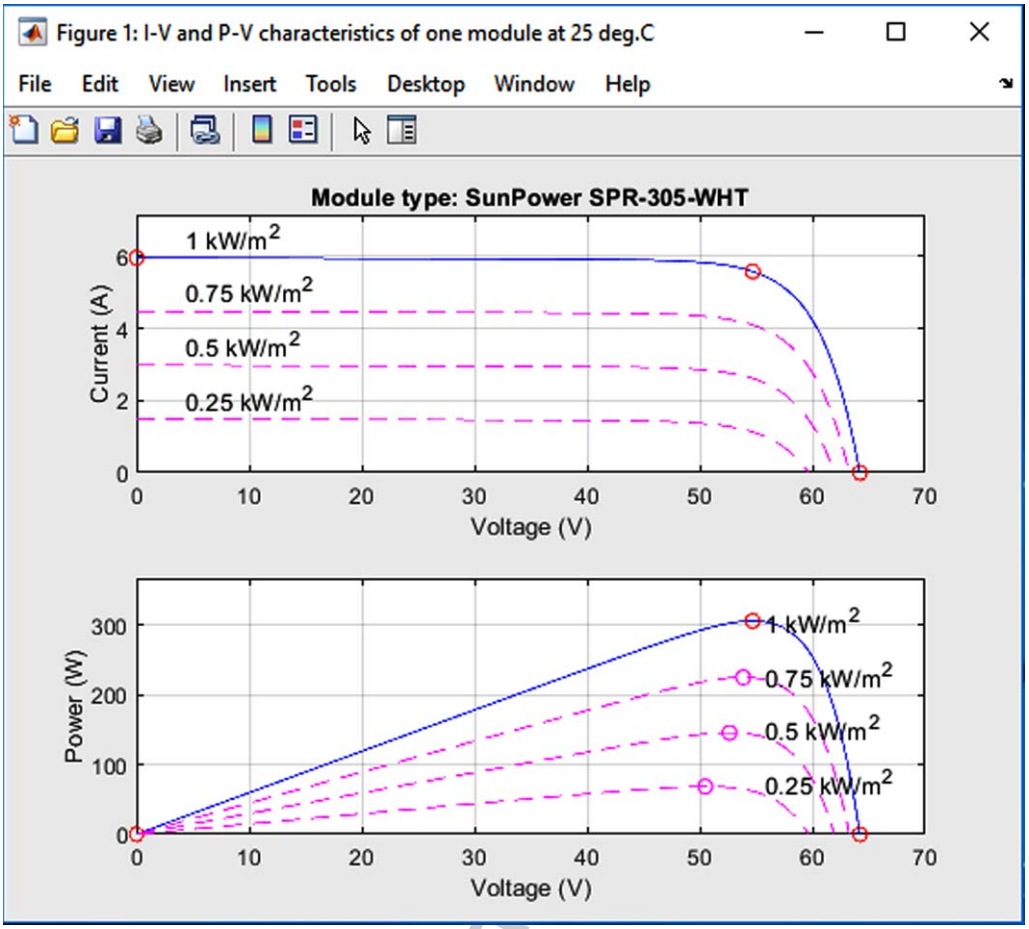


Fig. 3. Solar-PV Characteristics.

Table 2
Assessment of fifteen level traditional MLI

Different types of Multilevel Inverter (MLI)	Total Number of Stage	Number of Main diodes	Number of Switches	Number of clamping Diodes	Number of DC bus Capacitor	Number of Balancing Capacitors
Switched Capacitor-(MLI)		0	7	11	1	6
FC (MLI)		28	28	0	14	91
Binary Ladder- (MLI)		0	6	0	6	0
Modified Ladder- (MLI)		0	4	0	3	0
NPC (MLI)		28	28	182	14	0
CH-B (MLI)	15 level	28	28	0	7	0
Conventional (MLI)		3	12	6	3	0
Modular (MLI)		3	7	0	3	0
Switched Series/Parallel- (MLI)		6	14	0	3	1
Proposed (VL-MLI)		2	1	0	7	1

$V_{C1} = V_{DC}$ (input). The end result voltage V_{DC} (output) is highly elevated from input source voltage by the use of inductor (L1) and capacitor (C_1), when the during main switch off period (1-k) T decrease voltage level–(V_{out}–$2V_{DC\ input}$). Therefore ripple current of the inductor iL is given below. The equation can be given as,

$$\Delta iL_2 = \frac{V_1}{L_2} KT + \frac{V_{0-2V_1}}{L_2} I_{L1} (1 - K) T \quad (4)$$

$$V_1 = \frac{2 - K}{1 - K} V_{in} \quad (5)$$

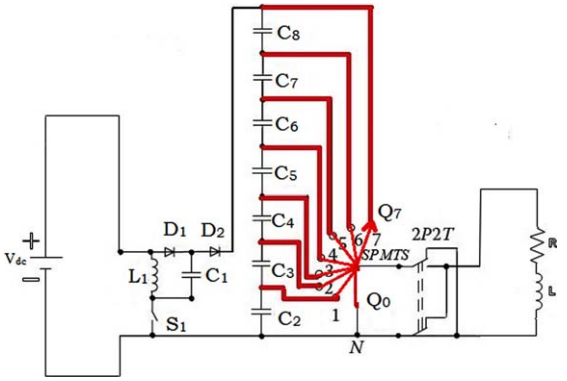


Fig. 4. ON-State VL-MLI.

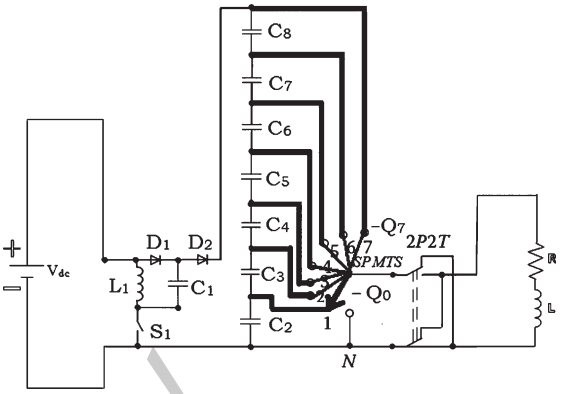


Fig. 5. OFF-State VL-MLI.

Where K is the Duty cycle.

The output voltage V_0, and the equation can be given as,

$$V_0 = \left(\frac{2-K}{1-K}\right)^2 V_{in} \quad (6)$$

3.1. ON – State (Positive Half cycle 0–180°)

The output voltage switch (Q7) position is a positively connected, when it is at the node D_2 and C_8, there is a potential voltage drop across the capacitor C_8, Which is named as $Q_7 = +1/7Vdc$, below this condition the double pole double through switch and the band switch position is closed as in Fig. 4. It is exact positively connected output voltage; the precise positive half cycle output voltage is appears in linear and nonlinear load. The exact switching position is clarified in the following steps:

- output voltage switch position $Q_6 = +1/6Vdc$, the voltage across the capacitor (VC_8 & VC_7) is appeared to double pole double through switch
- output voltage switch position $Q_5 = +1/5Vdc$, the voltage across the capacitor (VC_7 & VC_6) is appeared to double pole double through switch
- output voltage switch position $Q_4 = +1/4Vdc$, the voltage across the capacitor (VC_6 & VC_5) is appeared to double pole double through switch
- output voltage switch position $Q_3 = +1/3Vdc$, the voltage across the capacitor (VC_5 & VC_4) is appeared to double pole double through switch
- output voltage switch position $Q_2 = +1/2Vdc$, the voltage across the capacitor (VC_4 & VC_3) is appeared to double pole double through switch
- output voltage switch position $Q_1 = +1/1Vdc$, the voltage across the capacitor (VC_3 & VC_2) is appeared to double pole double through switch
- output voltage switch position $Q_0 = 0$, the voltage across the capacitor (VC_1) and neutral, it is appeared to double pole double through switch and band switch, that positive charging output will be passing appear to next stage of the linear and non-linear load.

3.2. OFF- State (Negative Half cycle 180°–360°)

The output voltage switch (-Q1) position is a negatively connected, when it is at the node C_2, there is a potential voltage drop across the capacitor C_8, Which is named as $-Q_1 = -1/1Vdc$, below this condition the double pole double through switch and the band switch position is closed as in Fig. 5. It is exact negative connected output voltage; the precise negatively charged half cycle output voltage is appears in linear and nonlinear load. The exact switching position is clarified in Table 3 and the following steps:

- output voltage switch position $-Q_2 = -1/2Vdc$, the voltage across the capacitor (VC_2 & VC_3) is appeared to double pole double through switch
- output voltage switch position $-Q_3 = -1/3Vdc$, the voltage across the capacitor (VC_3 & VC_4) is appeared to double pole double through switch
- output voltage switch position $Q_4 = -1/4Vdc$, the voltage across the capacitor (VC_4 & VC_5) is appeared to double pole double through switch
- output voltage switch position $-Q_5 = -1/5Vdc$, the voltage across the capacitor (VC_5 & VC_6) is appeared to double pole double through switch
- output voltage switch position $-Q_6 = -1/6Vdc$, the voltage across the capacitor (V_{C6} & V_{C7}) is appeared to double pole double through

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Table 3
Proposed VL-MLI switching

Capacitor bank single pole multi terminal Output voltage switch Point (SPMTS)	Total no. of Level	Switch ON State	Output voltage level expression	Capacitor bank single pole multi terminal output voltage switch Point (SPMTS)	Total no. of Level (Cont.,)	Switch OFF State	Time Band	Output Voltage (V)
Mode:1 (Q7)	1	+1/7Vdc	VC8	- Q7	15	-1/7Vdc	7 (5-sec)	30 V
Mode:2 (Q6)	2	+1/6Vdc	VC8 + VC7	-Q6	14	-1/6Vdc	6-7 (10 S)	60 V
Mode:3 (Q5)	3	+1/5Vdc	VC8 + VC7 + VC6	- Q5	13	-1/5Vdc	5-6-7 (15 S)	90 V
Mode:4 (Q4)	4	+1/4Vdc	VC8 + VC7 + VC6 + VC5	- Q4	12	-1/4Vdc	4-5-6-7 (20 S)	120 V
Mode:5 (Q3)	5	+1/3Vdc	VC8 + VC7 + VC6 + VC5 + VC4	- Q3	11	-1/3Vdc	3-4-5-6-7 (25 S)	150 V
Mode:6 (Q2)	6	+1/2Vdc	VC8 + VC7 + VC6 + VC5 + VC4 + VC3	- Q2	10	-1/2Vdc	2-3-4-5-6-7 (30 S)	180 V
Mode:7 (Q1)	7	+1/1Vdc	VC8 + VC7 + VC6 + VC5 + VC4 + VC3 + VC2	- Q1	9	-1/1Vdc	1-2-3-4-5-6-7 (35 S)	210 V
Mode:8 (Q0)	8	0	N	Q0	-	0	0 (N)	0

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switch. output voltage switch position in -Q_7 = -1/7Vdc, the voltage drop across the capacitor (V_{C7} & V_{C8}) is appeared to double pole double through switch, the voltage drop across the capacitor (V_{C7}), it is appeared to double pole double through switch and band switch, that negative charging output will be passing appear to next stage of the linear and non-linear load.

4. Harmonic elimination half height (H-H) method

The multilevel DC/AC Converters have various structures and many benefits. Unfortunately, most existing inverters are unable to produce good output sinusoidal waveforms because of their poor total harmonic distortion (THD) because each level switching angle is not carefully arranged. In order to the power quality (PQ) overall gain is properly investigate and switching angle arrangement to obtain the reduce lower order harmonics level [29]. The switching angle is the moment of the level change m-level (m is an odd number) waveform in the period (0°–90°), there are 2(m – 1) switching angles to be determined first quadrant period i.e., (0°–90°) as main switching angles as shown in Fig. 6. The switching angles are derived by in following the steps:

1. Switching angles in the first-quadrant VL-MLI (i.e., 0°–90°): $\alpha 1, \alpha 2 \ldots, \alpha(m-1)/2$.
2. Switching angles in the second-quadrant VL-MLI (i.e., 90°–180°): $\alpha(m+1)/2 = \pi - \alpha(m-1)/2, \ldots, \alpha(m-1) = \pi - \alpha 1$.
3. Switching angles in the third-quadrant VL-MLI (i.e., 180°–270°): $= \pi - \alpha\ \alpha m = \pi + \alpha 1 \ldots \alpha 3(m-1)/2 = \pi + \alpha(m-1)/2$.
4. Switching angles in the fourth-quadrant VL-MLI (i.e., 270°–360°): $\alpha(3m-1)/2 = 2\pi - \alpha(m-1)/2, \ldots, \alpha 2(m-1) = 2\pi - \alpha 1$.

Reduction of THD in the way of best switching angle can be divided in four types: Equal-Phase (EP) method, Half-Equal-Phase (HEP) Method, Half-Height (HH) Method, Feed-Forward (FF) method [30, 31]. The multilevel switching waveform can be determined by the above four methods. Unfortunately the EP, HEP, FF methods are looks very thin, like a triangle waveform arrangements and larger gaps between the positive half-cycle and the negative half-cycle. The proposed new H-H method is find best switching angle value in multilevel sinusoidal waveform, which is reduce THD in between both positive and negative half cycle with reduced gap. The main switching angles are in the ranges calculated from 0–2π.

Which are determined by the formula:

$$\boldsymbol{\alpha_i = Sin^{-1}\left[\frac{2i-1}{m-1}\right]} \tag{7}$$

Where $i = 1, 2, \ldots\ \frac{m-1}{2}$

Hence, the exits Harmonic Elimination (HE) by selection of switching angle is calculate a set of non-linear equations and its governing the amplitude of each individual harmonics obtain in offline mode [32]. HE technique is the most difficult to solve greatly increases levels of the MLI. The harmonic elimination techniques are determine by the line side harmonics and load side harmonics [33, 34], which is find the switching angle value and reduces harmonics level in VL-MLI. The proposed half height (H-H) method switching angles can be achieved by driving a number of mathematical non-Linear equations using for PSO algorithm. The VL-MLI is also the most famous single switching strategy, which is used to specifically eliminate the odd order harmonics from the output waveform of the multilevel inverter. Its produces output phase voltage with suitable switching angles. Furthermore, all traditional MLI presents odd harmonic levels are difficult to calculate. Even harmonics is a positive half cycle still left which does not have a negative half-cycle to cancel it. It is zero at the output of phase voltage. Hence, H-H method can use analysis function calculate the odd harmonics in the phase voltage is given by,

$$\boldsymbol{\alpha_{1,2,3,\ldots n}} = \sum_{i=1,2,3,\ldots n}^{m=15} i\frac{90^\circ}{\frac{m-1}{2}} = i\frac{180^\circ}{m-1} \tag{8}$$

$$\boldsymbol{\alpha_{1,2,3,\ldots n}} = \sum_{\boldsymbol{i}=1,2,3,\ldots \boldsymbol{n}}^{\boldsymbol{m}=15} \boldsymbol{i\frac{270^\circ}{\frac{m-1}{2}} = i\frac{360^\circ}{m-1}} \tag{9}$$

Therefore development of H-H method can use analysis best switching angles in the four quadrants (i.e., 0°–360°) and furthermore increasing the inverter levels. Calculate the lower order harmonics in the phase voltage Equations (8) and (9) are set to be zero and eliminate odd harmonics respectively. Modulation index (MI) represent the fundamental voltage is given as,

$$M = \frac{Vref}{Vj} \tag{10}$$

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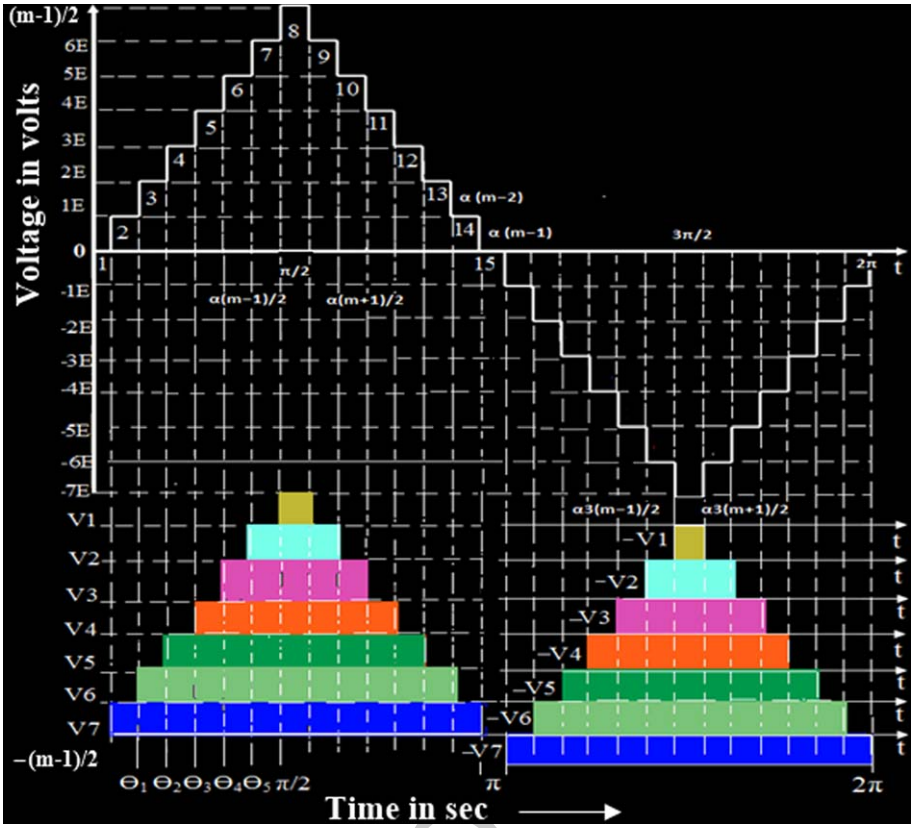


Fig. 6. Voltage Lift- Multilevel waveform of switching angle determination.

Considering the output voltage and amplitude of dc sources would be written as:

$$V_n = \sum_{n}^{\infty} v_n \sin(nwt) \tag{11}$$

Now optimal switching angles can be named as $\propto_1, \propto_2, \ldots .. \propto_n$ that found depend on modulation index. Thus, PSO algorithm can be programmed for finding the optimal switching value for eliminating THD and maintained their original voltage value.

5. Implementation of modified pso algorithm

Particles are flowing through the problem area by tracking the current optimum particles. Modified species-Based particle swarm techniques have been developed by [35] to determine the optimum switching angles for a multi-level converter and cannot be determined using either traditional iterative techniques or resulting theory method. The PSO techniques are producing required voltage with lower order harmonics [36], while minimize the objective function and investigate switching pattern of both bipolar and unipolar case.

Cascade five level MLI [37], to solve non-linear transcendental equation for different modulation Index and eliminate the lower order harmonics with less computational period. In recent [38], A single phase modified MLI have propounded, there are plenty of optimization techniques in the determination of switching angles, but PSO algorithm requires less time to calculate and minimizes the harmonics problems of the multilevel output waveform. The VL-MLI has also defined the method of H-H with reduced THD and to find switching angle with MPSO optimization algorithm. The original formulations that can boost its efficiency with the particles changes, according to the solving the harmonics optimization problems is as follows:

- PSO starts with assignment of initial velocity & particles.
- In each particle generate random locations, it evaluates the objective function to determine

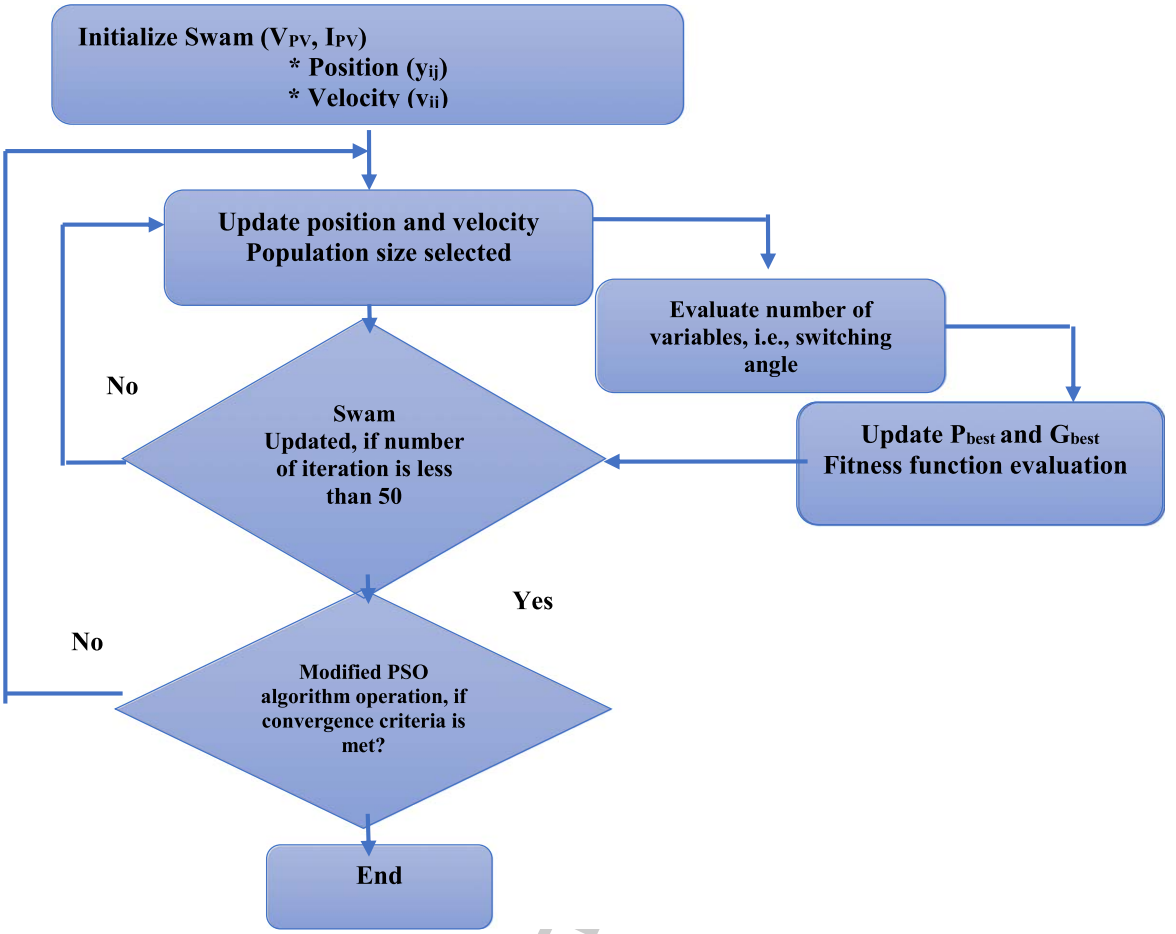


Fig. 7. Flowchart for MPSO implementation.

the best location value, and discard the same fitness value.

- PSO particles select new velocities based on the current velocity
- To determine the individual best locations with their neighbors.
- In MPSO, a group of random particles and then optimized by updating generations in each particle is updated with two best values, the best fitness values among all the particles chosen the each iteration.

Iterations proceed with the particles locations, velocities, and updates or adjust neighbors until the algorithm is reaches a stopping criterion as shown in Fig. 7. Modified PSO algorithms that differ in the size of their neighborhoods have been developed. The first one is G_{best} MPSO, for each particle the neighborhood is the entire swarm calculated in velocity (v) equation. Which particle swarm is the best optimizer value, and this value is called P_{best}. Another "best" value that is tracked by so far, where smaller neighborhood for each particle are defined as in the population, It is called as local best and it's denoted as L_{best}.

$$V_{ij} = V_{ij}(t) + C_1 R_1(t)\left[Y_{ij}(t) - X_{ij}(t)\right] + C_2 R_2 j(t)\left[Y_j(t) - X_{ij}(t)\right] \quad (12)$$

Where,

V_{ij} (t)- Velocity of the particle at a time (t),

Dimension; j-1, 2, ...N,

X_{ij}(t)- Position of the particle a time (t),

C_1, C_2 - Positive acceleration constants; R_1, R_2 - Random values, ranges from 0 to 1.

The personal best position, yi, associated with particle i is the best position visited by the particle, since the first step and the next time step (t + 1) calculated as,

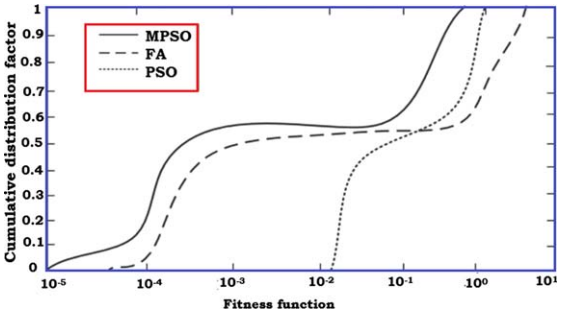


Fig. 8. Comparison of convergence rate (FA, PSO & proposed MPSO).

$$X(t+1) = X(t) + V(t+1) \tag{13}$$

Where each particle can expand the search criteria depend on the present best value, after finding the two best values, the particles are update velocity and positions with following equation (12) and (13). To verify the efficiency of the proposed system (MPSO) compare with CDF (cumulative distribution factor) [39, 40] and fitness values is find out in Fig. 8. The overall results are obtained and establishment of MPSO convergence rate was compared with PSO, and FA.

6. Simulation result and discussion

In this paper deals with 15-level VL-MLI support the MPSO algorithmic program using Proteus 7.7 Simulink code. This code must realize the optimum solution for the modulation index (MI), which depends on the VL-MLI transition angle. The single input supply (PV) is connected directly to series connected to a multilevel inverter voltage raise. This simulation of VL-MLI is conducted with the 50 Hz output frequency and a 3000 Hz transfer frequency. Figure 9 displays their respective VL-MLI electrical converter output voltage R, RL, and DC Voltage. Figure 10 shows their respective capacitor unit output voltage across the each individual capacitor C_2 to C_8. The MPSO is a much higher achievement level economically to find the best switching angle for the different load Vs THD level presented in Table 4. The ranges of MI differ from 0.1 to 0.1 for corresponding switching angles are calculated using the given PSO formula (section 4). The parameters are shown in PSO algorithm maximum particles 20, maximum iteration 100 and number of swarm 150. The swarm's velocity and position has been quit updated and the optimal solution has been found with minimum interval time. The required switching angles are efficiently calculated by dynamic inertia weight PSO algorithm for the entire modulation index. Its shows the optimum switching angle value as shown in Fig. 11 (a). Figure 11 (b) shows the best switching angle versus MI for modified PSO optimized VL-MLI. The speed of convergence MPSO approach for obtaining very high value, and it's to eliminate harmonics by using H-H method. Swarm optimization has no issue to associate with Genetic Algorithm (GA) and Firefly Algorithm (FA). PSO optimization to find the globally optimized

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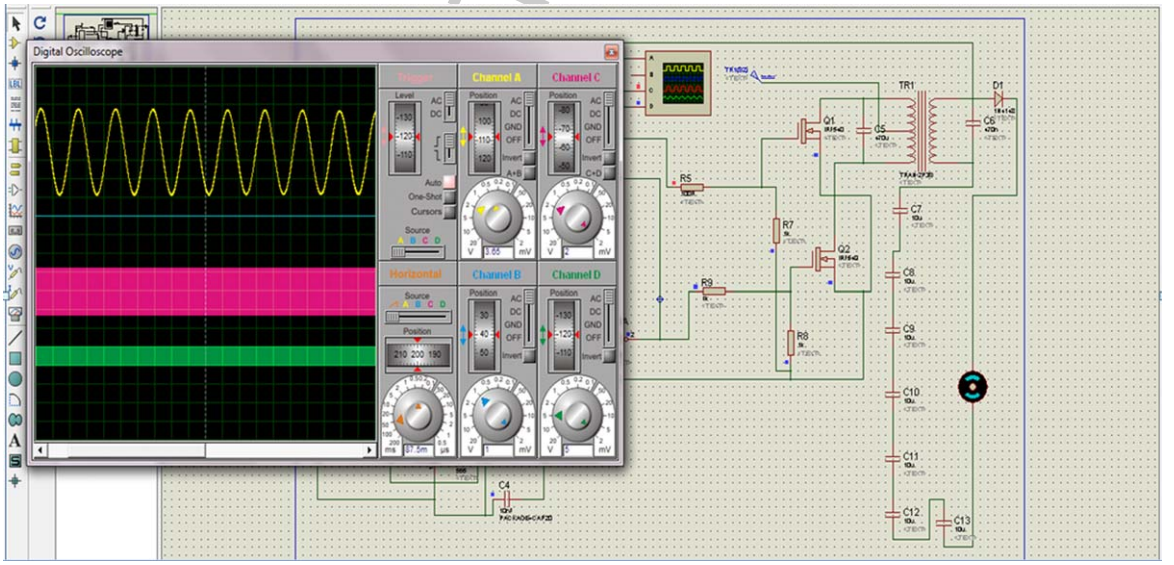


Fig. 9. Output voltage of 15- level VL-MLI.

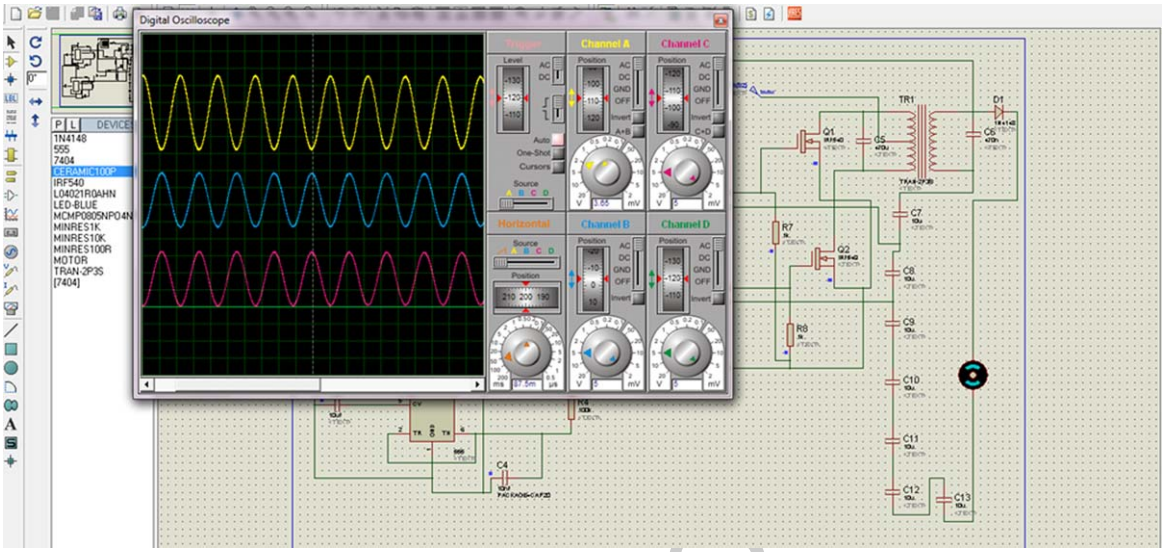


Fig. 10. Different capacitor unit output voltages in VL-MLI.

Table 4
PSO control parameters

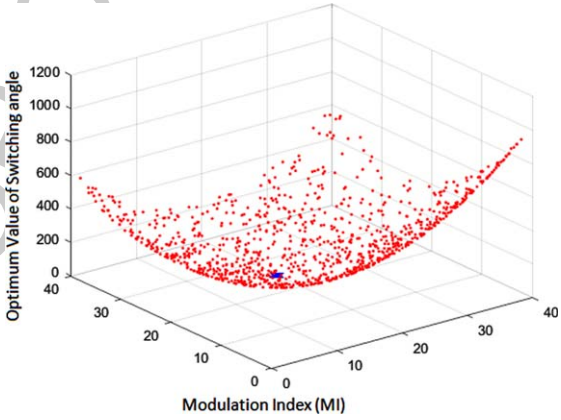
Parameters	Value
Inertia weight, *w*	09 ~ 0.3
Random Values [R_1, R_2]	[0,1]
No. of particles	40
Max. Iteration	100
Cognitive factor, C_1	0.02
Social factor, C_2	0.91
Time Taken	2
No. of population	40
Best modulation Index	0.8
Optimum switching angle	$\alpha_1 = 18.95$, $\boldsymbol{\alpha_2 = 23.50}$, $\alpha_3 = 53.91$, $\alpha_4 = 66.91$, $\alpha_5 = 66.91$, $\alpha_6 = 66.91$, $\alpha_7 = 66.91$.

solution with both GA and FA are discussed. The linear (R-load), non-linear (RL-load) harmonic distortion levels are decreased using MPSO and H-H methods shown in Fig. 12 (a&b).

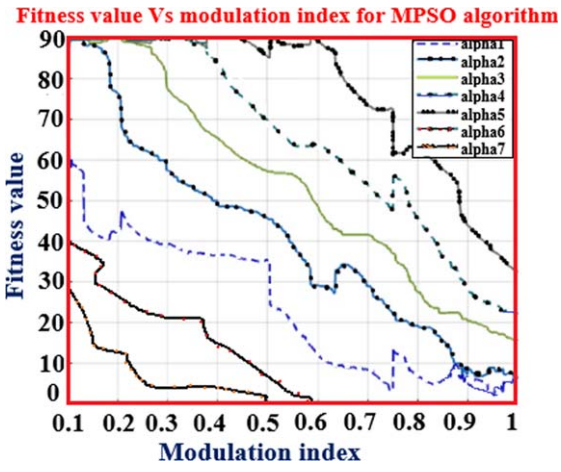
The improvements of reactive power (VAR) are varied in R&RL load. It's eliminating negative sequence current in inverter output with the help of a series capacitor unit in order to maintain system balance. The proposed VL-MLI output reduced harmonics are presents in 0.95% (R load) and 1.35% (RL load) as shown in Table 5.

7. Hardware results and discussion

The selected operating points in correspondence with the simulation results are developed for the hard-

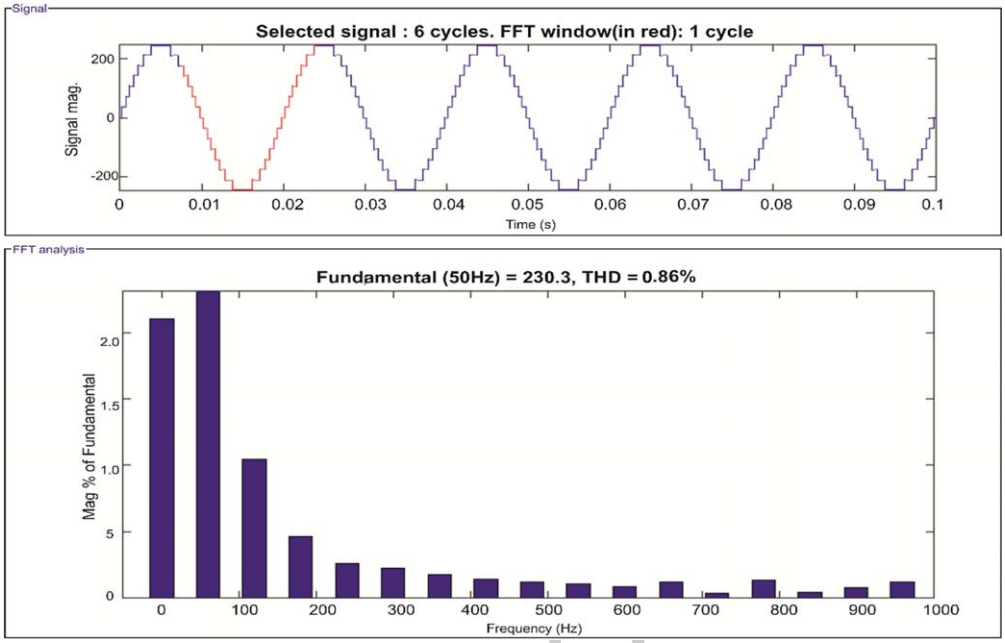


(a)

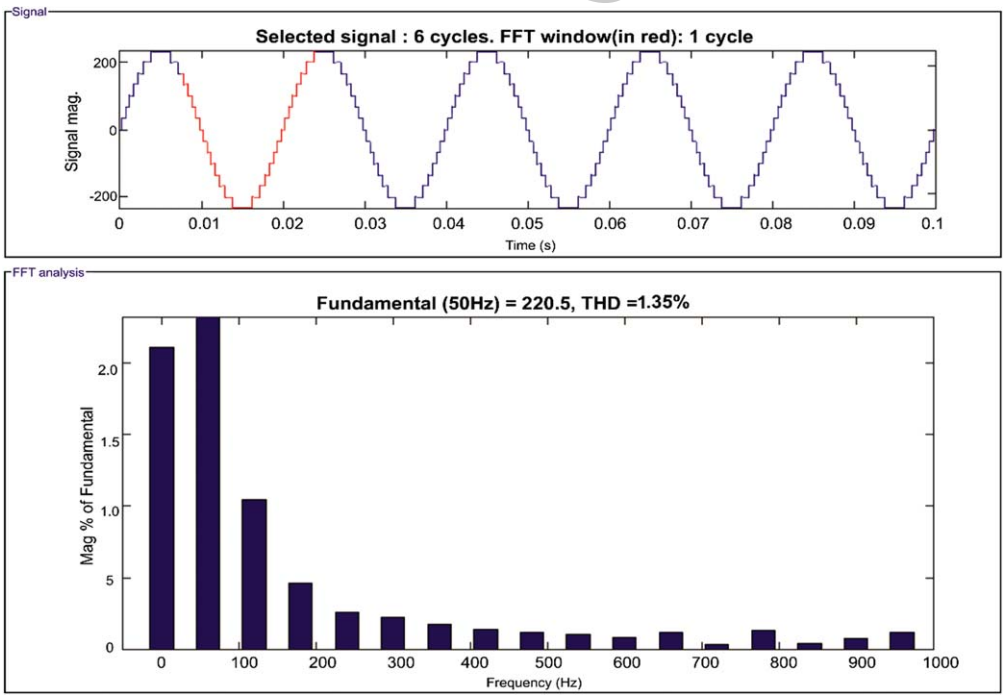


(b)

Fig. 11. (a) Optimum switching angle using for PSO algorithm. (b) Calculating switching angle (α_1 to α_7).



(a)



(b)

Fig. 12. (a) Proposed MPSO using VL-MLI (R load). (b) Proposed MPSO using VL-MLI (R load).

ware verification. Four PV sting connected single PV module are used in the experimental setup as shown in Fig. 13. The load resistance of the prototype is to R = 90Ω, RL = (Stator resistance 10Ω, Rotor resistance 5.3Ω, Stator inductance 0.464 H, Rotor inductance 0.461 H, and solar PV sources switching frequency is 1-4 KHz. The experimental setup is operating and associated with the help of FPGA-

Table 5
Comparison of results with the existing topologies

Authors	Techniques	Level	THD%
A. Routray et al. (2019) [41]	MPSO	11	9.85% (R load)
Thenmalar Kaliannan et al. (2021) [21]	PSO	15	11.72% (RL load)
Vivek Kumar Gupta et al. (2016)	PSO	7	17.5% (RL load)
A. Iqbal et al., (2019) [3]	GA	11	12.75% (RL load)
J R Albert et al. (2020) [10]	FA	15	6.85% (R load)
J R Albert et al. (2020) [10]	FA	15	4.35% (RL load)
Thenmalar Kaliannan et al (2021) [21]	PSO	15	7.40% (R load)
A. Routray et al. (2019) [41]	MPSO	11	5.85% (RL load)
Proposed VL-MLI	**MPSO**	**15**	**0.86% (R Load)**
	MPSO	**15**	**1.35% (RL Load)**

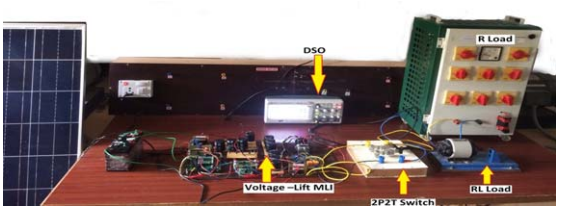


Fig. 13. Hardware setup for FPGA 3-AN Kit tuned Modified PSO algorithm.

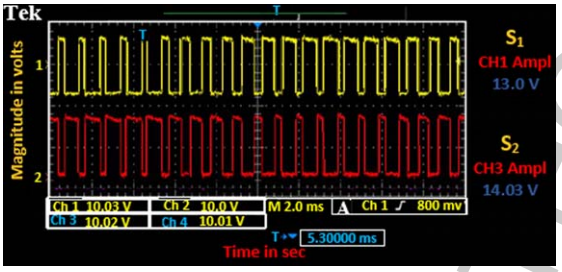


Fig. 14. Gate pulse and modulation signals using Xilinx Spartan 2-AN kit.

Xilinx Spartan 2AN kit with battery step up. The PSO assist VHDL code into FPGA proposed model were presented. The performances of gate pulse and modulation signals are given PSO rules through Xilinx Spartan 2AN kit as shown in Fig. 14. The operating parameters are used in the simulation and experimental low-power model almost the same.

The system design voltage-lift multilevel inverter output is 210 V, 1.5 A, operated with an output frequency of 50 Hz, and a carrier switching frequency of 10,000 Hz as shown in Fig. 15 (a&b). The VL-MLI control with the respective standalone mode in order to deliver a multilevel output voltage waveform of 15 levels is almost sinusoidal, which is confirming the effectiveness of this modulation strategy. This prototype model of VLMLI is turning on MOSFET-IRF710PBF through the voltage in series and along with series capacitor unit (1500μF) or VL-MLI capacitor bank C_2-C_8. The first positive half cycle is made up with SPST switch and double pole double through (2P2T) switching unit. The performance gate signal is given through buffer from Xilinx Spartan 2AN kit and the SPMT switch is on condition, at same time 2P2T switch close the position of (Q_0 to Q_7) & (-Q_7 to –Q_1) respectively.

8. Conclusion

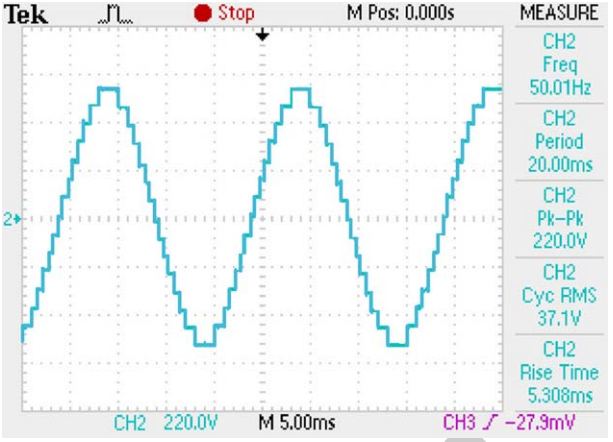
In this proposed context, modified PSO optimizations get a handle on approach in simulation, and prototype FPGA model with least distortion output voltage. The P-Q priority are used to apply 15- level MLI. The performance measures of the asymmetric multilevel productivity voltage waveform, such as harmonic distortion values are studied, and contrast is made by appropriate values. VL-MLI minimum harmonics presence is 0.85% (R load) and 1.5% (RL load). A prototype single phase circuit with less switching stress and low distortion output was verified successfully. In the coming decades, the proposed MLI circuit will be a great choice for power electronic frameworks, particularly for photovoltaic and wind power applications.

Declaration of interest

Funding

This research has not received any funding support.

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(a)



(b)

Fig. 15. (a) Output voltage. (b) Experimental output harmonic anlaysis.

Conflict of interest

Authors are declare that, there is no conflict of interest.

Ethical approval

This article does not contain any studies with human participants or animals performed by any of the authors.

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